

ATT7030A

Application Note

Directory

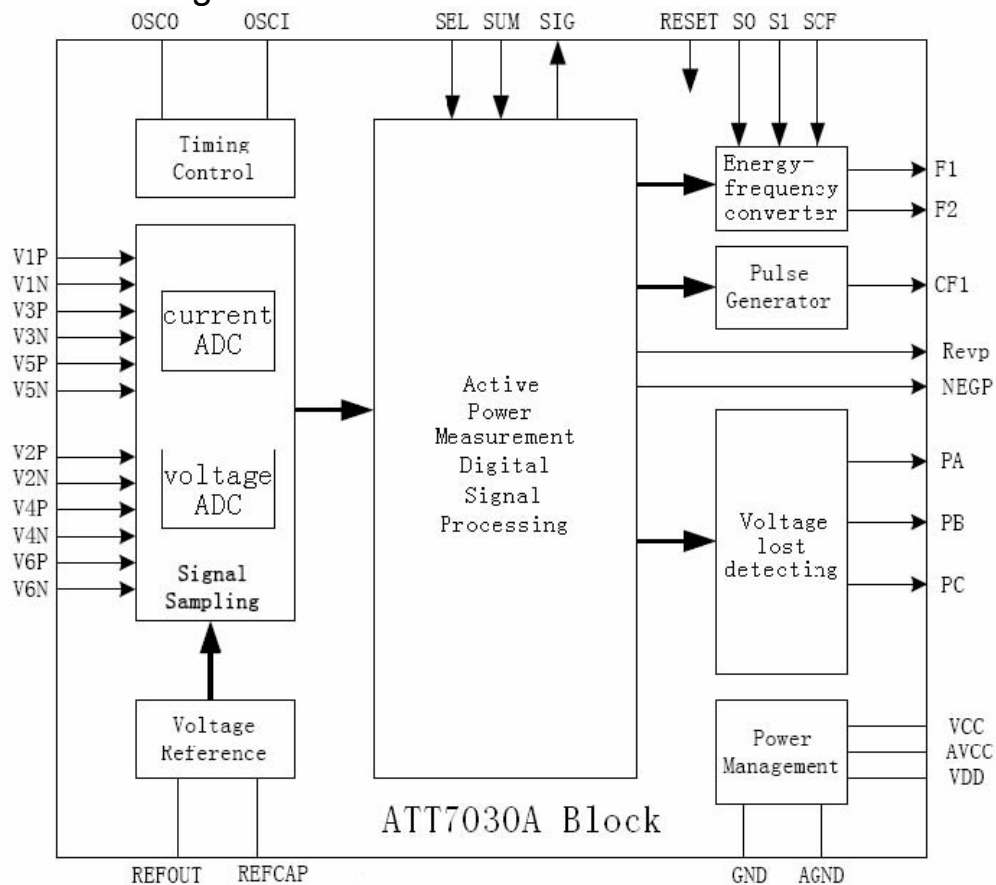
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This application note describes the implementation of a multifunctional three-phase energy meter using the ATT7030A. Please peruse ATT7030A's user manual before reading this application note.

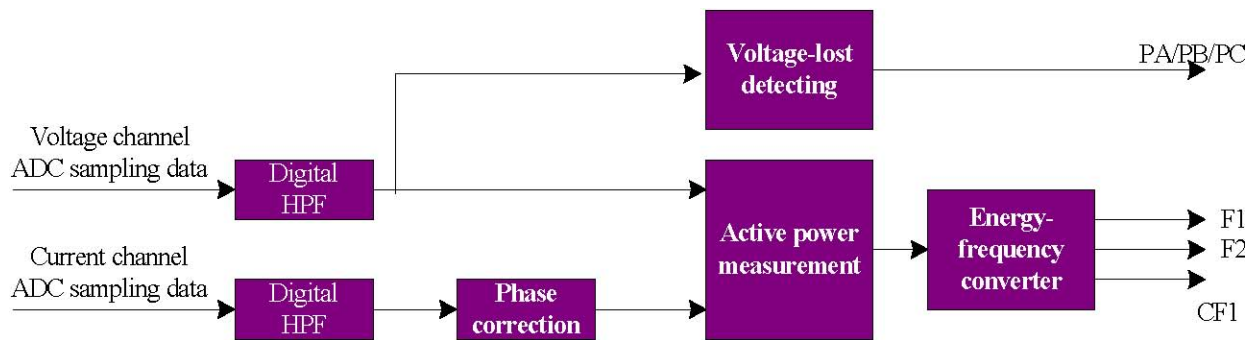
ATT7030A features:

- Active energy measure accord with IEC 62053-21;
- Selectable calculation mode for 3-phase energy combined (algebraic addition or absolute addition);
- Provide high-frequency energy pulse output;
- Provide pulse output F1/F2 for driving electromechanical counter and stepper motor;
- Provide voltage-lost detected for every phase;
- Provide negative power indication REVP when any one phase active power is negative;
- Provide negative phase indication (NEGP) when 3-phase combined power is negative;
- Compatible with 3-phase 3-wire and 3-phase 4-wire;

The internal block diagram in ATT7030A:



The signal disposal flow chart:



ATT7030A's package is QFP44. The external hardware circuitry includes power supply, voltage and current analog signal input, pulse output and electromechanical counter.

Analog input circuitry

ATT7030A incorporates 6 second-order 16-bits ADCs. The voltage sampling data is 0.2V ~ 0.6V. The current sampling data is 2mV ~ 1V. The energy linear error is less than 0.1%.

Every ADC's AC signal is input from VxP and VxN. At the same time the VxP and VxN need be added 2.4V direct current bias voltage, which could be obtained from ATT7030A's reference voltage output 'REFOUT' or external benchmark voltage.

ATT7030A's sampling input voltage can adopt resistance divided-voltage method (as diagram 1 and diagram 2), or switching voltage to current, then through current mutual inductance implement switching current to voltage (as diagram 3). The latter method adopt mutual inductance implement, which can segregate chip and electric power net, thereby can get favorable anti-jamming capability. In diagram 1, the neutral line Vn is connected to reference voltage output 'REFO', which achieves adding AC sampling signal to 2.4V direct current bias voltage expediently. In diagram 2, the neutral line Vn is connected to chip's ground, which is applied to power supply using autotransformer.

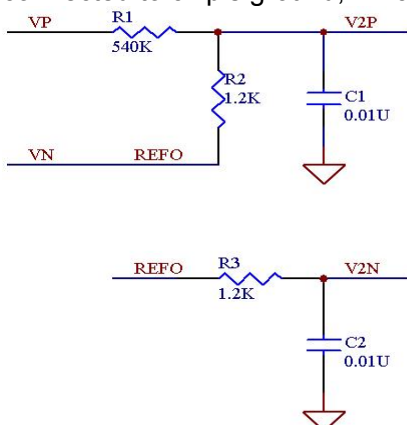


Diagram 1: Vn is connected to REFO

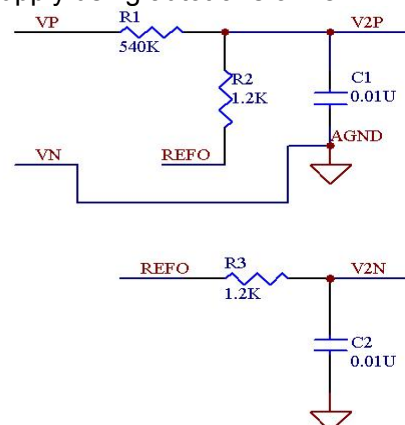


Diagram 2: Vn is connected to ground

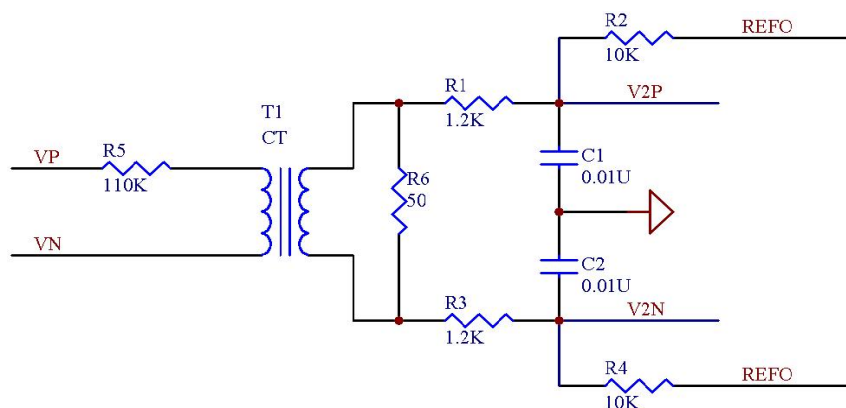


Diagram 3: current mutual inductance

In the above diagram, VP and VN are connected to phase line and neutral line, the relevant parameter correspond to 220V voltage. In diagram 3, the CT's transformation ratio is 1:1.

CT achieves ATT7030A's sampling input current. There have nether connection method.

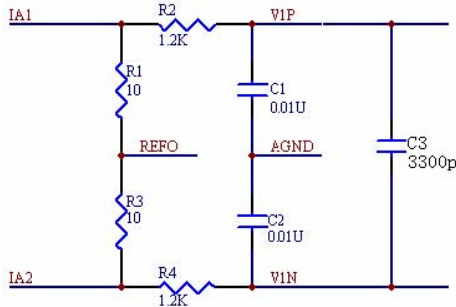


Diagram 4 current sampling differences input

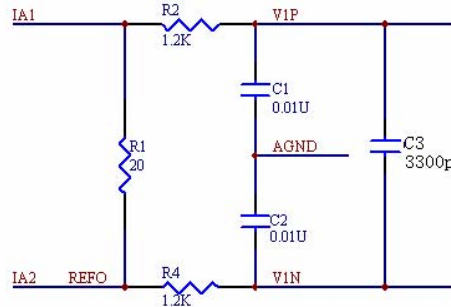


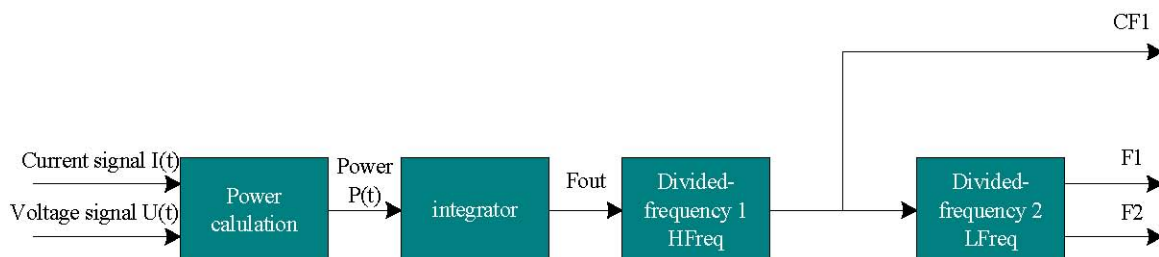
Diagram 5 current sampling single-port input

In diagram 4 and diagram 5, IA1 and IA2 is CT's secondary signal.

We should notice some points when design sampling input signal:

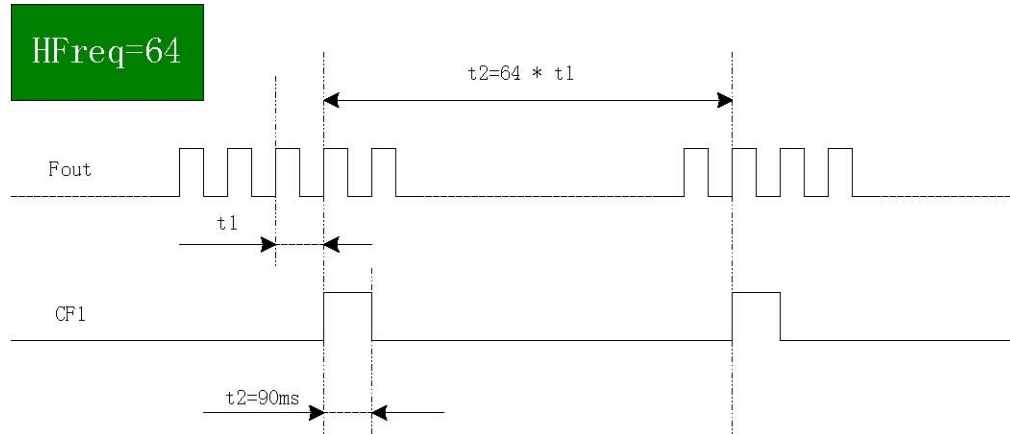
1. Whatever input method, the direct current bias voltage of input pin VxP and VxN should be 2.4V. The bias voltage must be provided by pin REFOUT (pin 11), or else the measurement precision couldn't be assured.
2. For assuring measurement precision, the capacitance filter (10uF and 0.1uF) connected to pin 5 should be closer to the best to pin 5, furthermore any one can not be left out. The grounding point of capacitance and ground of sampling signal must be shorted.
3. In VxP and VxN input circuitry, 1.2K resistance and 0.01uF capacitance make up of antialiasing filter, whose structure and parameter should be symmetrical. For attaining favorable temperature characteristic, we should adopt well component in temperature capability.
4. In sampling input circuitry, capacitance C3 (3300pF) is used to regulate phase error, whose magnitude should be decided by actual phase error.
5. Default start-up current value is 0.1mV (0.1%Ib).
6. In 3 phase 4 wire mode, voltage-depreciation threshold voltage is 75mV (15%Vn); in 3 phase 3 wire mode, voltage-depreciation threshold voltage is 300mV (60%Vn).
7. When any one phase current is reversed to voltage, the pin 40 (REVP) would output high level. Base on this we can judge the correctness of connection.
8. SEL pin connected to high level denotes 3 phase 4 wire connection method; low level denotes 3 phase 3 wire connection method.
9. The 3-phase 3-wire meter adopts two-component measurement method. In this condition SEL is selected to low level, VB substitutes VN in connection interface. The voltage sampling input V4P/V4N and current sampling input V3P/V3N can become unaided signal input.
10. When 3-phase energy addition mode selects algebraic addition, NEGP can output direction indication basing on the sign of 3-phse power algebraic additions. Using this function, we can make stop-reverse 3-phase energy meter convenient.

Energy pulse output circuitry

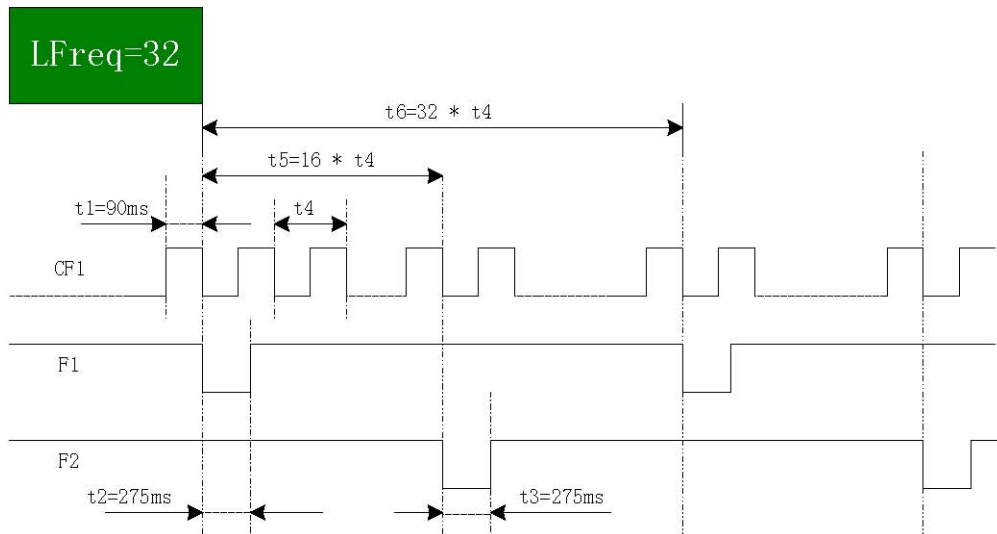


In power measurement signal processing circuitry, switched voltage and current signal multiply to get hold of instantaneous power, which integrating to the time to turn into energy. A/B/C phase energy is summated according to algebraic addition mode or absolute addition mode basing on input pin SUM, through switching the result to frequency signal and divided-frequency, then we get hold of energy pulse output signal which could be used to calibrate. On this foundation, divided-frequency again can get hold of low-frequency pulse output signal which could be used to drive stepper motor.

Underside is divided-frequency sketch map when high-frequency output constant is 64. The pulse-width of energy pulse output is 90ms. When pulse cycle is less than 180ms, energy pulse output duty cycle is 1 : 1.



Underside is divided-frequency sketch map when low-frequency output constant is 32. The pulse-width of energy pulse output (F1/F2) is 275ms. When pulse cycle is less than 550ms, energy pulse output duty cycle is 1 : 1.



How to select appropriate pulse constant and electromechanical counter ratio? In other words, how to select SCF/S1/S0?

If we use CF to denote the frequency of calibration pulse, then

$$CF = 1600 \cdot V_u \cdot V_i \cdot G \cdot H_{freq} \quad (1)$$

Thereinto V_u is input voltage on the voltage sampling pin (V2P and V2N, V4P and V4N, V6P and V6N) in rated voltage condition; V_i is input voltage on the current sampling pin (V1P and V1N, V3P and V3N, V5P and V5N) in rated current condition. $G = 0.648$ (correspond to 2.5V reference voltage). H_{freq} is high-frequency output constant.

On the other hand, $CF = N \cdot U_n \cdot I_b / 3600000 \quad (2)$

Thereinto N is pulse constant (calibration constant), U_n is rated voltage, I_b is rated current.

Follow above two formula, $Hfreq = 5760000000 * Vu * Vi * G * G / (N * Un * Ib)$ (3)

By usually, Vi is 0.1V; Vu (0.2V ~ 0.6V) is selected to make $Hfreq$ close to the value in List-1 basing on Un , Ib and pulse constant N .

List-1

SCF	S1	S0	Hfreq	Lfreq
0	0	0	256	16
0	0	1	128	16
0	1	0	128	8
0	1	1	128	4
1	0	0	64	16
1	0	1	64	8
1	1	0	64	4

$Lfreq$ is divided-frequency coefficient for driving electromechanical counter. The ratio of electromechanical counter should be:

$$N/Lfreq * 2 \quad (4)$$

Give a example: design a 3 phase 4 wire meter, the rated voltage is 220V, rated current is 5A, then how to select pulse const? How to select ratio of electromechanical counter? How to select SCF/S1/S0? How much is the sampling voltage in voltage loop?

Step 1: suppose $Vu = 0.5V$, $Vi = 0.1V$, by formula 3:

$$Hfreq = 5760000000 * 0.5 * 0.1 * 0.648 * 0.648 / (220 * 5 * N) \\ = 109938 / N$$

Then $N = 109938 / Hfreq$

Hfreq	256	128	64
N	429	858	1717

So pulse constant can be selected as 429 ~ 1717. Calibration pulse would be faster along with pulse constant's augment, which can shorten calibration time in feeble-signal. Pulse constant can be selected as 400, 800, or 1600 after switched to integer; corresponding $Hfreq$ is 256, 128, 64.

If pulse constant is selected as 320, then sampling voltage = $0.5 * 320 / 429 = 0.37V$, at this time corresponding $Hfreq$ is still 256.

Step 2: select ratio of electromechanical counter

Basing on List-1, if $Hfreq = 256$, then $Lfreq = 16$, so ratio = $400 / 16 * 2 = 50$, SCF/S1/S0 = 0/0/0. If pulse const is 320, then ratio is 40.

If $Hfreq = 128$, $Lfreq$ can be selected as 16, 8, or 4. When $Lfreq = 16$, ratio = $800 / 16 * 2 = 100$, SCF/S1/S0 = 0/0/1. When $Lfreq = 8$, ratio = $800 / 8 * 2 = 200$, SCF/S1/S0 = 0/1/0. When $Lfreq = 4$, ratio = $800 / 4 * 2 = 400$, SCF/S1/S0 = 0/1/1.

If $Hfreq = 64$, $Lfreq$ can be selected as 16, 8, or 4. When $Lfreq = 16$, ratio = $1600 / 16 * 2 = 200$, SCF/S1/S0 = 1/0/0. When $Lfreq = 8$, ratio = $1600 / 8 * 2 = 400$, SCF/S1/S0 = 1/0/1. When $Lfreq = 4$, ratio = $1600 / 4 * 2 = 800$, SCF/S1/S0 = 1/1/0.

Step 3: calculate sampling voltage Vu

By usually, CT achieves ATT7030A's sampling input current. Connect appropriate resistance at CT's secondary coil can make $Vi = 0.1V$. By formula (3):

$$Vu = Hfreq * N * Un * Ib / (5760000000 * Vi * G * G) \\ = 64 * 1600 * 220 * 5 / (5760000000 * 0.1 * 0.648 * 0.648)$$

$$= 0.4657V$$

This value is in 0.2V ~ 0.6V, accords with the design requirement.

When Hfreq is made certain, sampling voltage would be smaller along with pulse constant N's smaller.

Step 4: select divided-voltage resistance

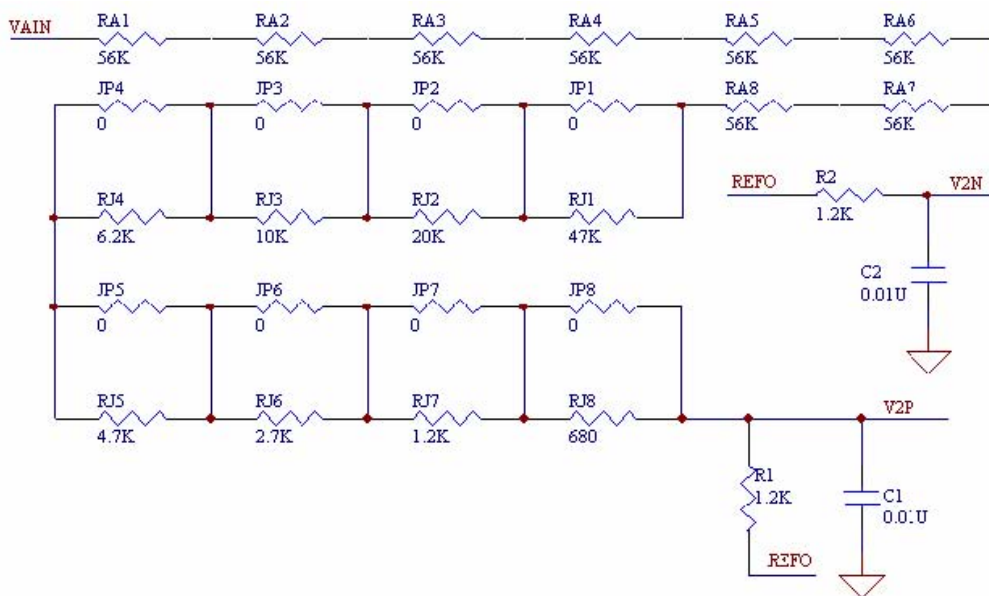
Select divided-voltage need consider nether factor: (1) consumed power; (2) voltage resistance of divided-voltage; (3) adjustable error range.

Basing on antialiasing filter's parameter demand in voltage loop, we suggest that the connected to ground resistance in voltage loop is 1.2K, then divided-resistance = $220 \times 1.2 / 0.4657 = 566K$. Considering reference voltage' difference in actual application, we should reserve 25% adjustable range, so sampling resistance is selected in 450K-560K, thereinto 450K is aptotic resistance and about 110K is adjustable resistance.

Considering double over-voltage capability, aptotic resistance need endure 400V voltage. If every resistance's over-voltage capability is 50V (please refer to the technique parameter of resistance), then we need eight aptotic resistances and the value is $450 / 8 = 56K$. If minimal adjustable precision is 0.1%, then minimal adjustable resistance could be 680Ω.

Adjustable resistance	680	1.2K	2.7K	4.7K	6.2K	10K	20K	47K
Adjustable precision	0.1%	0.2%	0.4%	0.8%	1%	2%	4%	9%

The nether circuitry is sampling voltage input, which uses resistance divided-voltage method.



We should notice some points when design energy pulse output signal:

1. Select appropriate level of input pin SUM.

If SUM is connected to high level, then:

In 3-phase 4-wire mode, 3-phase energy's calculation uses algebraic addition.

In 3-phase 3-wire mode, 3-phase energy's calculation uses absolute addition.

If SUM is connected to low level (default), then:

In 3-phase 4-wire mode, 3-phase energy's calculation uses absolute addition.

In 3-phase 3-wire mode, 3-phase energy's calculation uses algebraic addition.

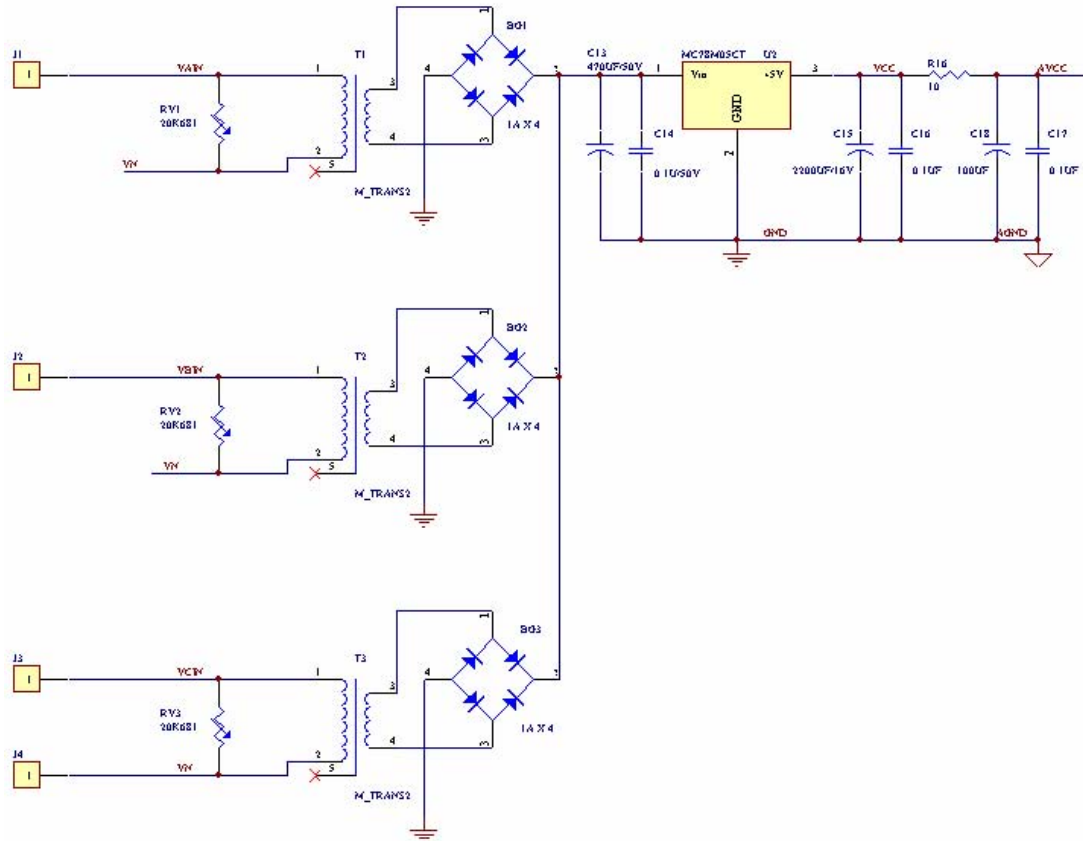
2. If stepper motor is used to output signal, F1 and F2 ports should be connected to resistance- capacitance filter.

3. Connect 1000p ~10nF decoupling capacitance nearly at energy pulse output port CF1.

The latter two points can achieve favorable electromagnetism compatibility.

Power supply circuitry

This is 3-phase power supply **circuitry schematics**:



The design of power supply circuitry is greatly important to energy meter's capability. For assuring favorable electromagnetism compatibility, we should notice nether points:

1. Power supply voltage VCC and AVCC don't exceed $5V \pm 5\%$ as specified for normal operation.
2. The output port of 7805 is connected 2200uF filter capacitance.
3. GND and AGND are digital and analog ground reference point. In PCB layout they should be connected to great area ground handy. For assuring low resistance characteristic of ground, GND and AGND shouldn't be differentiated and connected inductance, resistance, magnetic core element.
4. Great area ground layout cannot be put to front of commutating element. Underside of the fixed resistance of voltage sampling cannot be laid ground. Strong electricity and week electricity must be detached.
5. VN should connect voltage- hypersensitive resistance, and then connect to chip's internal circuitry.

ATT7030A work state whether or not right

How to judge ATT7030A's work state whether or not right after power up? We should check it from nether points:

1. IC voltage. VCC and AVCC should be loaded 5V voltage after power up. VDD (pin 33 and pin 39) is brought by the ATT7030A, and is 3.0V in working order. Pin 5 is internal reference voltage. Pin 11 is reference voltage output, used for providing current bias voltage for external input circuitry. The normal voltage of this two pin is 2.3V ~ 2.7V, which is brought by the ATT7030A.
2. Crystal surge frequency: 24.576MHz. Check the frequency and amplitude.
3. RESET (pin 1) is high level when ATT7030A is normal. If RESET is low level, denotes the

ATT7030A is in reset state.

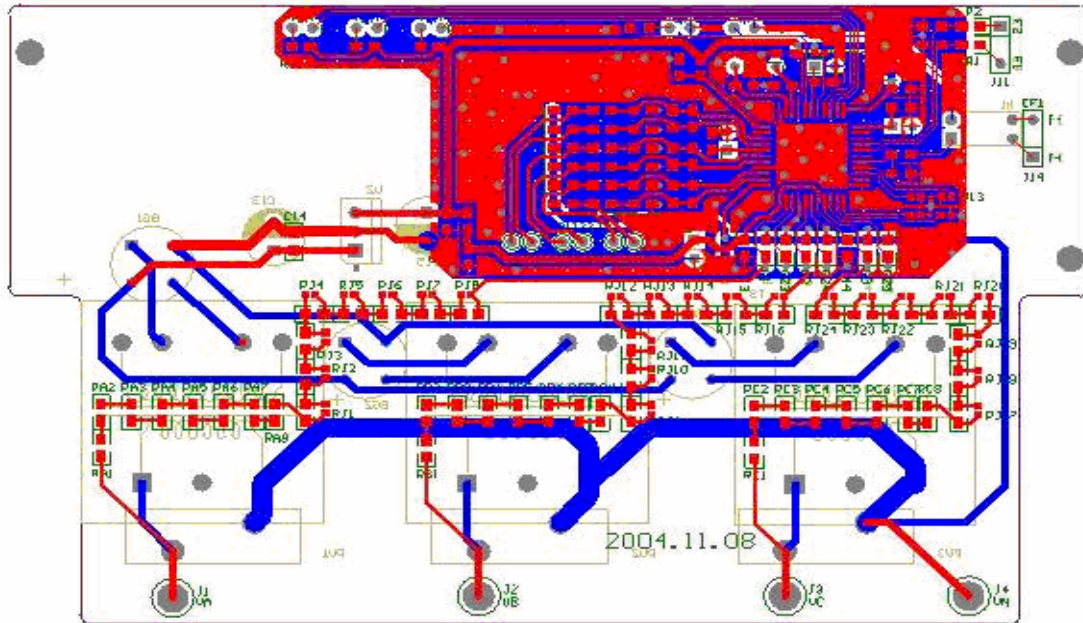
4. SIG should be low level all along.

Above signals are normal denotes the ATT7030A is in working order, or else we should check connection, short circuit and false jointing etc.

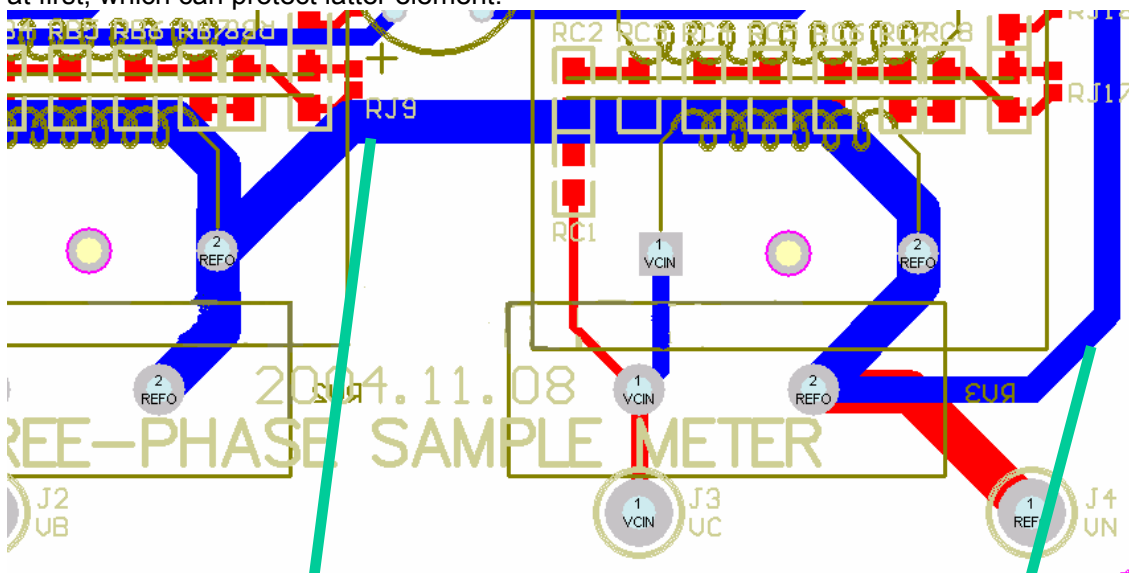
PCB layout

We use nether PCB for ATT7030A to explain fundamental for ATT7030A's PCB layout.

1. First of all, strong electricity and week electricity must be detached in PCB layout.



2. Phase line, neutral line and REFOUT pin should be connected to voltage- hypersensitive resistance at first, which can protect latter element.

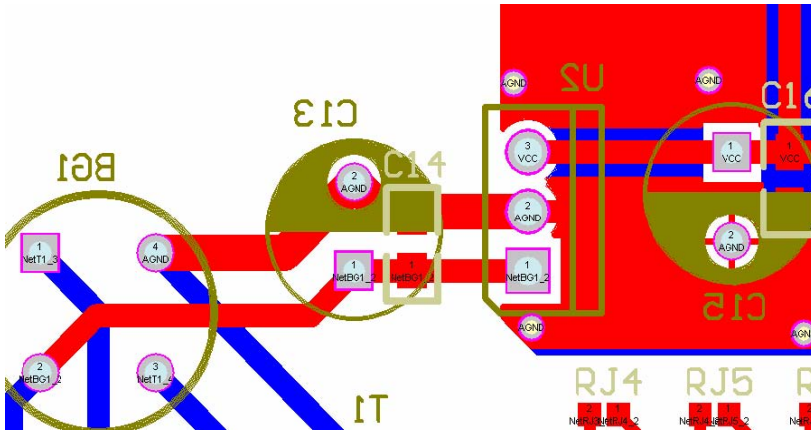


Note①

Note②

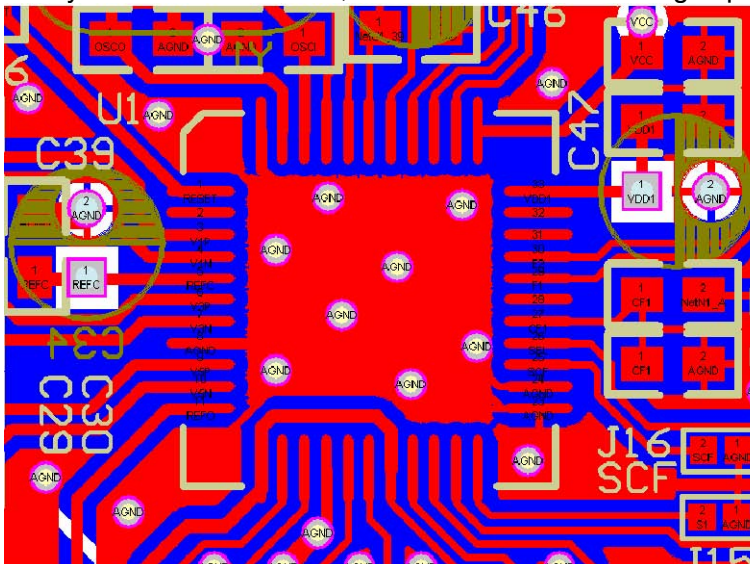
- ① The connect line of neutral line and voltage-hypersensitive resistance should be as thick as possible to absorb disturbance.
- ② In resistance network divided-voltage circuitry, the connect line's breadth of neutral line and internal circuitry should exceed 1mm.

3. Ground connection is very important to electromagnetism compatibility. Notice the connect points of power supply ground and signal ground.



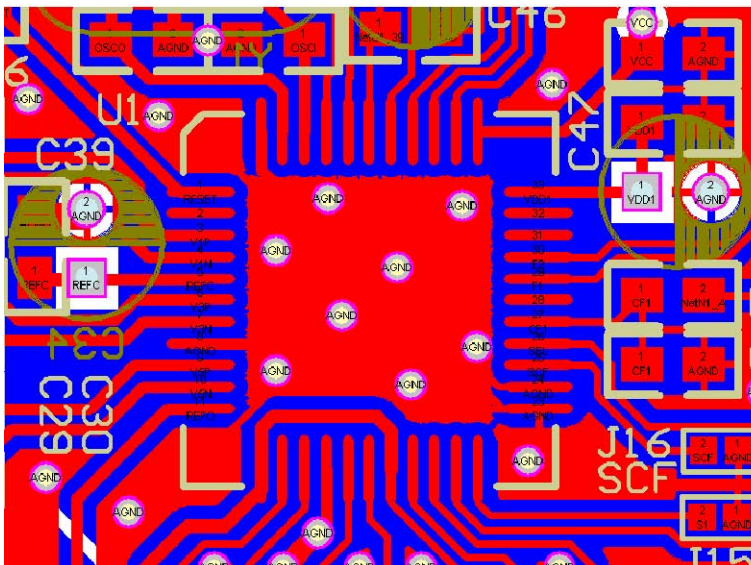
The power supply input of manostat module and GND should be connected at one point, so that disturbance in power supply can not arrive at whole system.

4. In PCB layout, the digital ground and analog ground should be connected to great area ground handy to reduce resistance, inductance and distributing capacitance in ground.



The GND and AGND are connected to whole ground. Assure ground's great area, integrity and low-resistance.

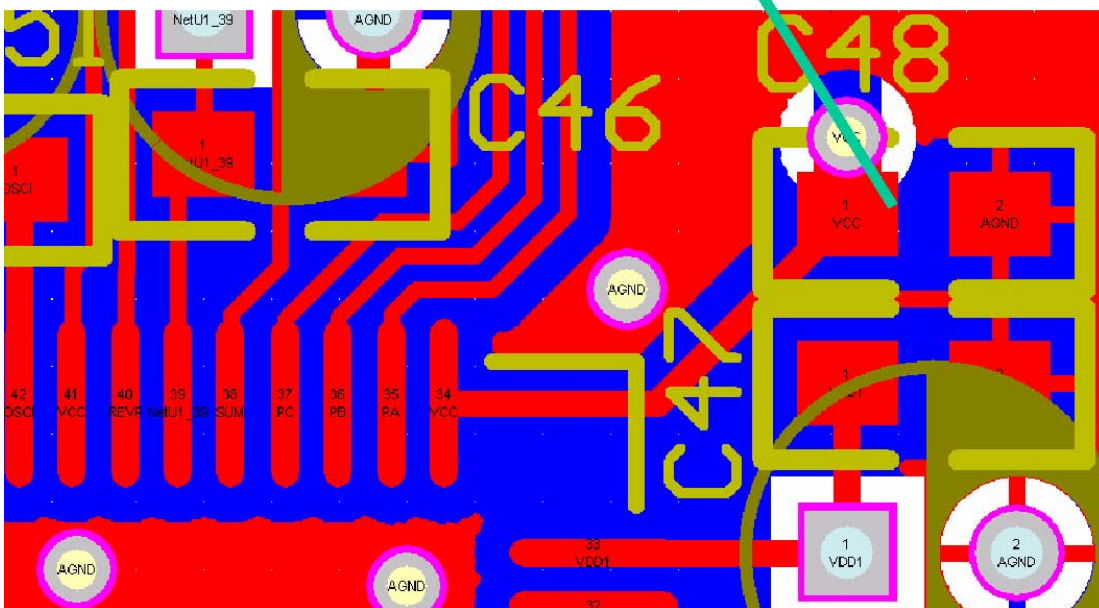
4. In PCB layout, the digital ground and analog ground should be connected to great area ground handy to reduce resistance, inductance and distributing capacitance in ground.



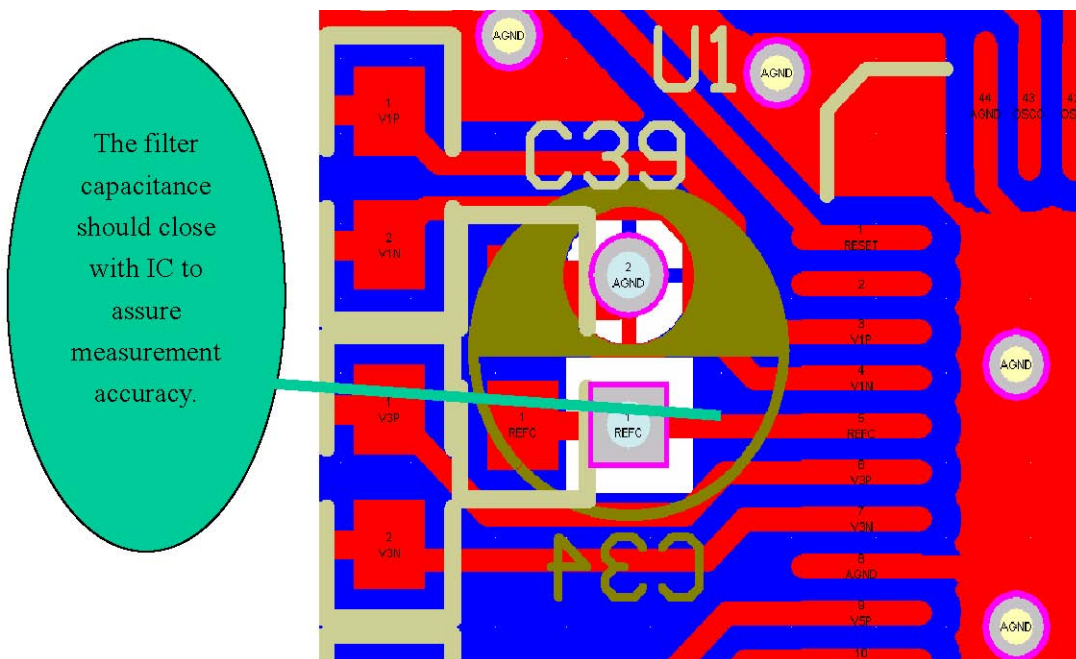
The GND and AGND are connected to whole ground. Assure ground's great area, integrity and low-resistance.

5. Notice the position of filter capacitance at the ATT7030A's power supply pin.

The filter capacitance of power supply should close with power supply pin to make signal through filter capacitance to IC's pin.
The breadth of line shouldn't be thin.

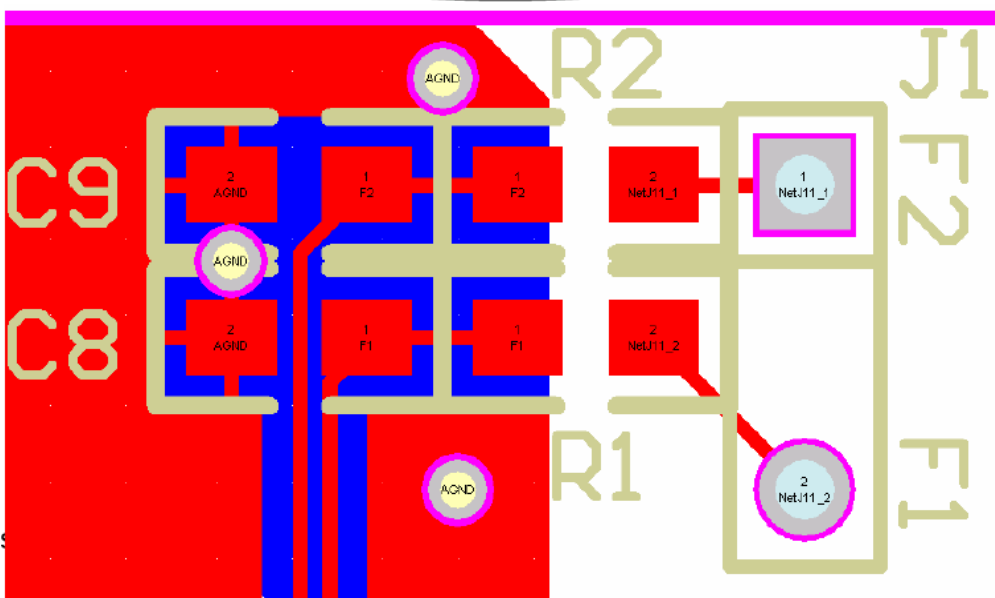


6. REFCAP pin should be connected filter capacitance, which can improve stability of reference voltage.

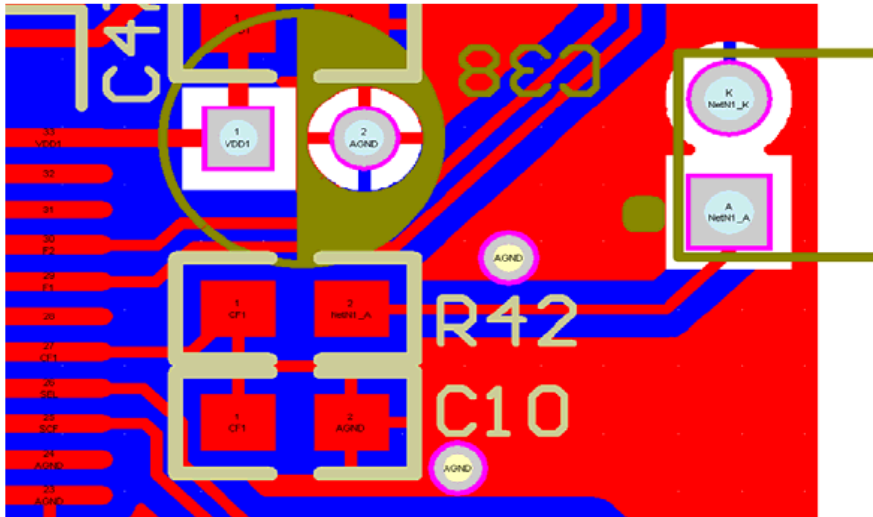


- 7 In high frequency radicalization area, the winding and magnet in stepper motor could be regarded as antenna, so filter circuitry should be used in signal line of driving stepper motor.

Resistance-capacitance filter can protect chip's stepper motor output port. Notice that the line should be as shorter as possible and be enveloped by ground line. The resistance and capacitance should be near to stepper motor's connect point.



- 8 As usually, the line of high frequency energy output pulse is very long, so decoupling capacitance is needed.



This capacitance can absorb disturbance and should be nearby to the ATT7030A.

- 9 Crystal oscillator is high frequency element, so its' neighborhood should be laid great area ground and avoid other signal line to traverse.

The curst of crystal oscillator should be connected to ground to assure the surge don't be disturbed.

