FAIRCHILD SEMICONDUCTOR®

July 2010

# FDFME2P823ZT

## Integrated P-Channel PowerTrench® MOSFET and Schottky Diode
## -20 V, -2.6 A, 142 mΩ

### Features

- Max $r_{DS(on)}$ = 142 mΩ at $V_{GS}$ = -4.5 V, $I_D$ = -2.3 A
- Max $r_{DS(on)}$ = 213 mΩ at $V_{GS}$ = -2.5 V, $I_D$ = -1.8 A
- Max $r_{DS(on)}$ = 331 mΩ at $V_{GS}$ = -1.8 V, $I_D$ = -1.5 A
- Max $r_{DS(on)}$ = 530 mΩ at $V_{GS}$ = -1.5 V, $I_D$ = -1.2 A
- Low profile: 0.55 mm maximum in the new package MicroFET 1.6x1.6 **Thin**
- **Schottky:** $V_F$ < 0.57 V @ 1A
- Free from halogenated compounds and antimony oxides
- HBM ESD protection level > 1600 V (Note 3)
- RoHS Compliant

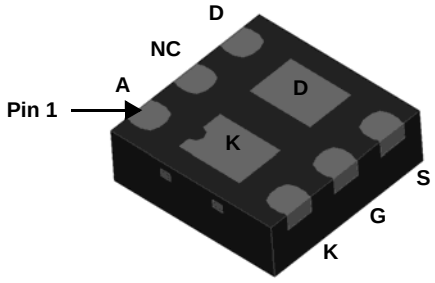
### General Description

This device is designed specifically as a single package solution for the battery charge switch in cellular handset and other ultra-portable appliacrions. It features as MOSFET with low on-state resistance and an independently connected low forward voltage schottky diode for minimum condution losses.

The MicroFET 1.6x1.6 **Thin** package offers exceptional thermal performance for it's physical size and is well suited to switching and linear mode applications.

### Applications

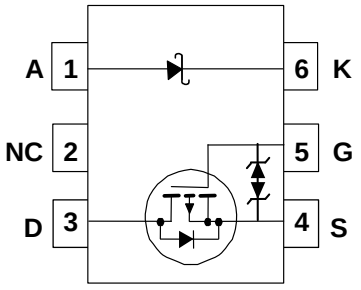
- Battery Charging
- DC-DC Conversion




BOTTOM



TOP




**MicroFET 1.6x1.6 Thin**

## MOSFET Maximum Ratings $T_A$ = 25 °C unless otherwise noted

| Symbol | Parameter | | | Ratings | Units |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | | -20 | V |
| $V_{GS}$ | Gate to Source Voltage | | | ±8 | V |
| $I_D$ | Drain Current -Continuous | $T_A$ = 25 °C | (Note 1a) | -2.6 | A |
| | -Pulsed | | | -6 | |
| $P_D$ | Power Dissipation for Single Operation | $T_A$ = 25 °C | (Note 1a) | 1.4 | W |
| | Power Dissipation for Single Operation | $T_A$ = 25 °C | (Note 1b) | 0.6 | |
| $V_{RRM}$ | Schottky Repetitive Peak Reverse Voltage | | | 28 | V |
| $I_O$ | Schottky Average Forward Current | | | 1 | A |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | (Note 4) | -55 to +150 | °C |

### Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Single Operation) | (Note 1a) | 90 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Single Operation) | (Note 1b) | 195 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Single Operation) | (Note 1c) | 110 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Single Operation) | (Note 1d) | 234 | |

### Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| 3T | FDFME2P823ZT | MicroFET 1.6x1.6 **Thin** | 7 ” | 8 mm | 5000 units |

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## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = -250 μA, $V_{GS}$ = 0 V | -20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = -250 μA, referenced to 25 °C | | -12 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = -16 V, $V_{GS}$ = 0 V | | | -1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±8 V, $V_{DS}$ = 0 V | | | ±10 | μA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = -250 μA | -0.4 | -0.6 | -1.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = -250 μA, referenced to 25 °C | | 2 | | mV/°C |
| $r_{DS(on)}$ | Drain to Source On Resistance | $V_{GS}$ = -4.5 V, $I_D$ = -2.3 A | | 95 | 142 | mΩ |
| | | $V_{GS}$ = -2.5 V, $I_D$ = -1.8 A | | 120 | 213 | |
| | | $V_{GS}$ = -1.8 V, $I_D$ = -1.5 A | | 150 | 331 | |
| | | $V_{GS}$ = -1.5 V, $I_D$ = -1.2 A | | 190 | 530 | |
| | | $V_{GS}$ = -4.5 V, $I_D$ = -2.3 A, $T_J$ = 125 °C | | 128 | 190 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = -4.5 V, $I_D$ = -2.3 A | | 7 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = -10 V, $V_{GS}$ = 0 V, f = 1 MHz | | 305 | 405 | pF |
| $C_{oss}$ | Output Capacitance | | | 55 | 75 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 50 | 75 | pF |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = -10 V, $I_D$ = -1 A, $V_{GS}$ = -4.5 V, $R_{GEN}$ = 6 Ω | | 4.7 | 10 | ns |
| $t_r$ | Rise Time | | | 4.8 | 10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 33 | 53 | ns |
| $t_f$ | Fall Time | | | 16 | 29 | ns |
| $Q_g$ | Total Gate Charge | $V_{DD}$ = -10 V, $I_D$ = -2.3 A, $V_{GS}$ = -4.5 V | | 5.5 | 7.7 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | | | 0.6 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | | 1.4 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = -0.9 A (Note 2) | | -0.8 | -1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = -2.3 A, di/dt = 100 A/μs | | 16 | 29 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 4.4 | 10 | nC |

### Schottky Diode Characteristics

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $I_R$ | Reverse Leakage | $V_R$ = 28 V | $T_J$ = 25 °C | | 15 | 100 | μA |
| | | | $T_J$ = 85 °C | | 0.46 | 4.7 | mA |
| $V_F$ | Forward Voltage | $I_F$ = 1 A | $T_J$ = 25 °C | | 0.47 | 0.57 | V |
| | | | $T_J$ = 85 °C | | 0.45 | | |
| $V_F$ | Forward Voltage | $I_F$ = 500 mA | $T_J$ = 25 °C | | 0.38 | 0.48 | V |
| | | | $T_J$ = 85 °C | | 0.33 | | |

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## Electrical Characteristics

**Notes:**

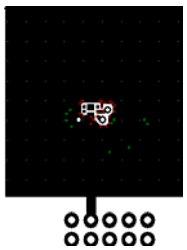
1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

   (a) MOSFET $R_{\theta JA}$ = 90 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB.

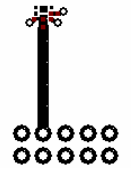
   (b) MOSFET $R_{\theta JA}$ = 195 °C/W when mounted on a minimum pad of 2 oz copper.

   (c) Schottky $R_{\theta JA}$ = 110 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper, 1.5 " x 1.5 " x 0.062" thick PCB.

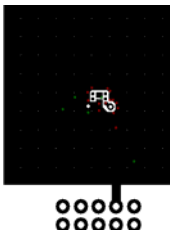
   (d) Schottky $R_{\theta JA}$ = 234 °C/W when mounted on a minimum pad of 2 oz copper.



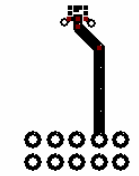
a. 90 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper.



b. 195 °C/W when mounted on a minimum pad of 2 oz copper.



c. 110 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper.



d. 234 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

4. Rating is applicable to MOSFET only.

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

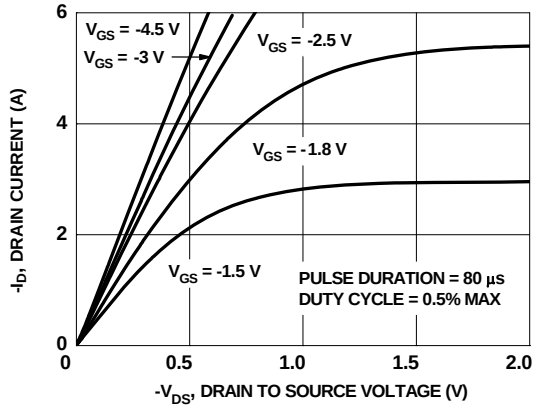



**Figure 1. On Region Characteristics**

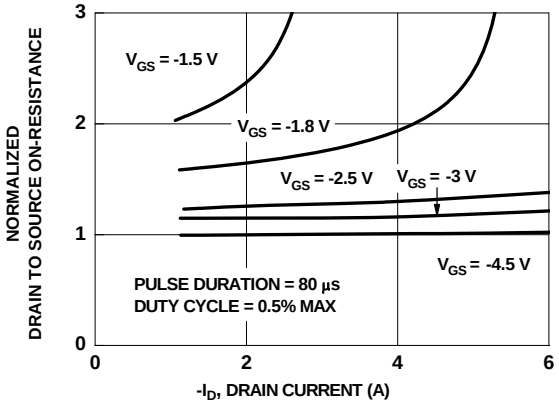



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

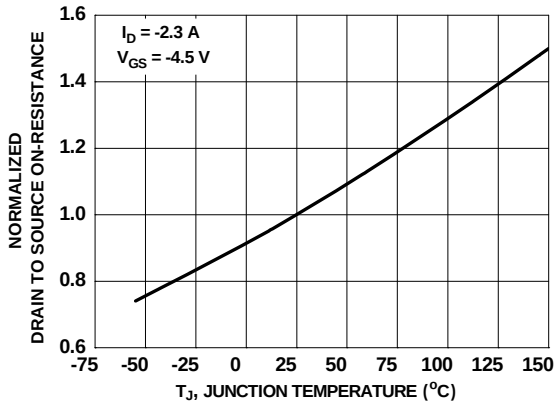



**Figure 3. Normalized On Resistance vs Junction Temperature**

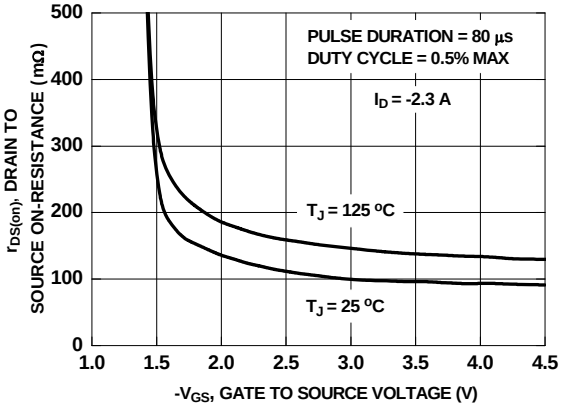



**Figure 4. On-Resistance vs Gate to Source Voltage**

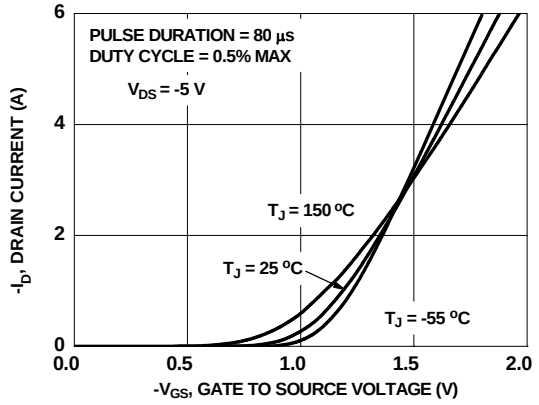



**Figure 5. Transfer Characteristics**

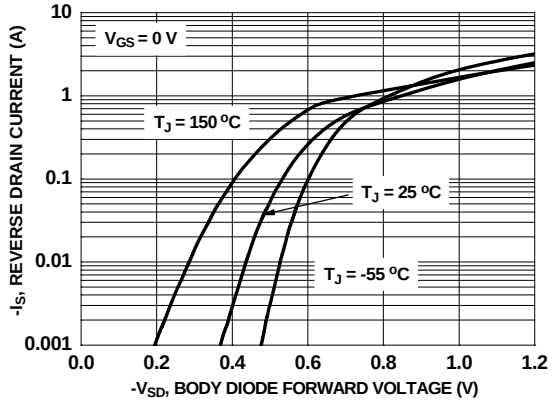



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

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## Typical Characteristics $T_J$ = 25°C unless otherwise noted

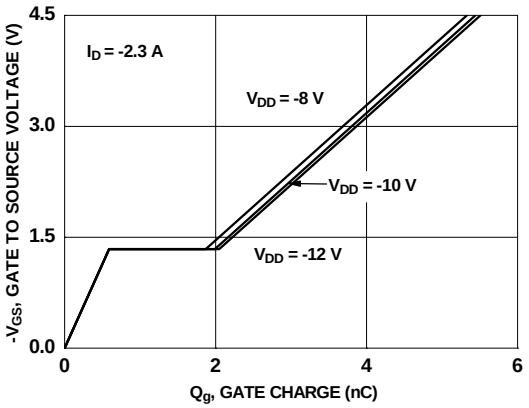



**Figure 7. Gate Charge Characteristics**

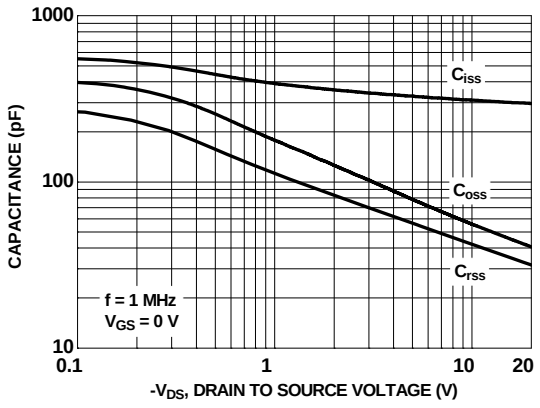



**Figure 8. Capacitance vs Drain to Source Voltage**

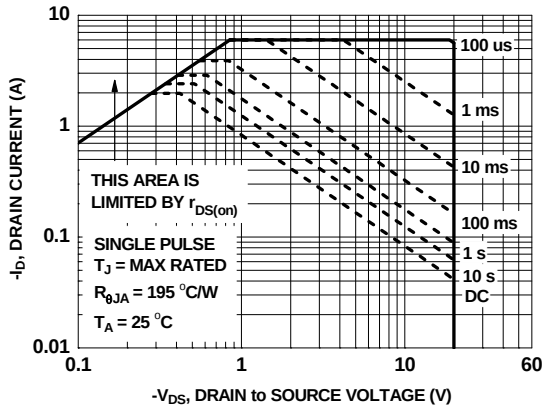



**Figure 9. Forward Bias Safe Operating Area**

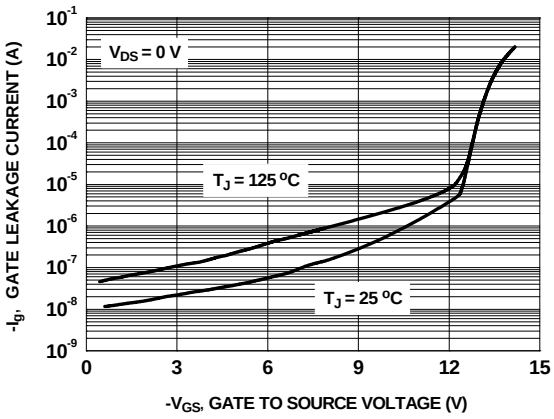



**Figure 10. Gate Leakage Current vs Gate to Source Voltage**

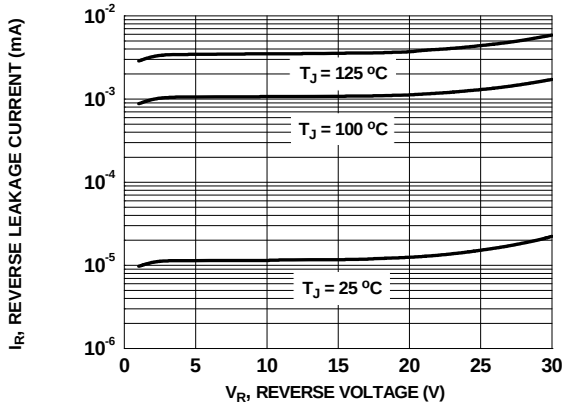



**Figure 11. Schottky Diode Reverse Current**

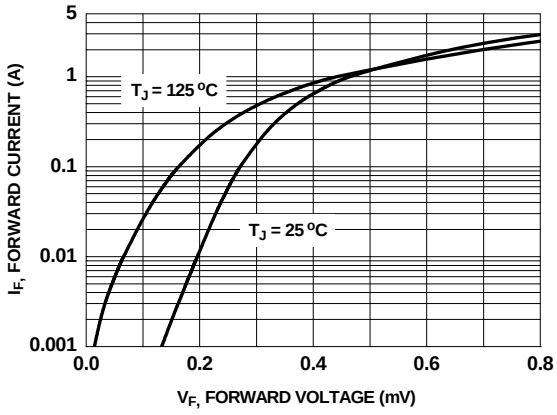



**Figure 12. Schottky Diode Forward Voltage**

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## Typical Characteristics $T_J$ = 25°C unless otherwise noted

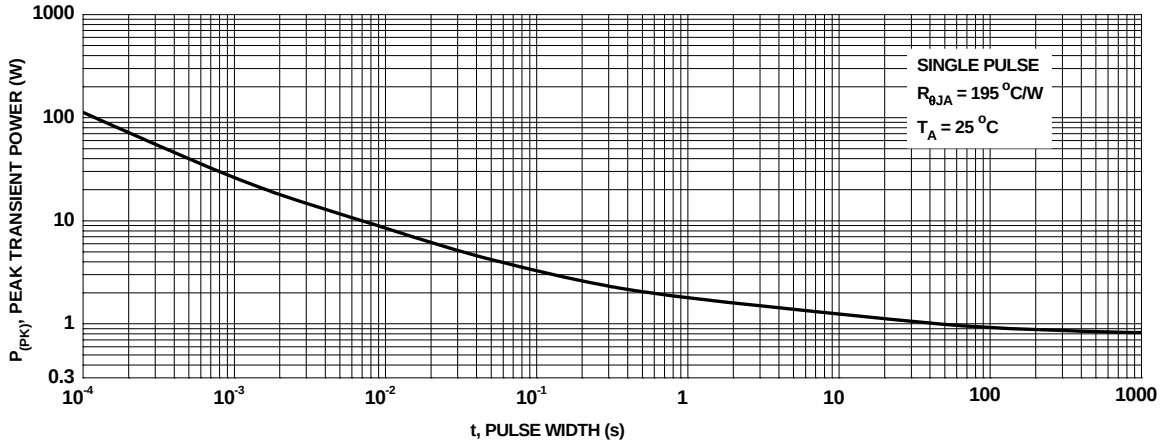



**Figure 13. Single Pulse Maximum Power Dissipation**

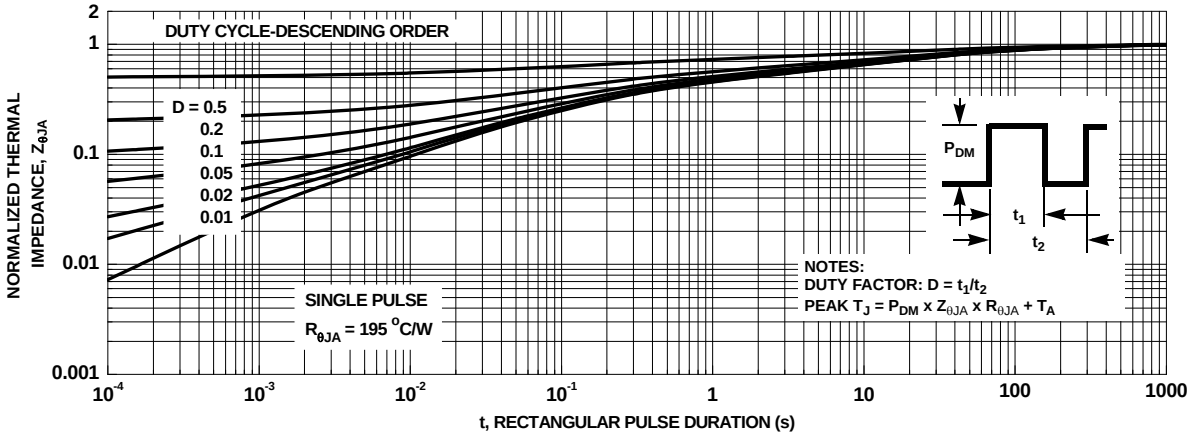
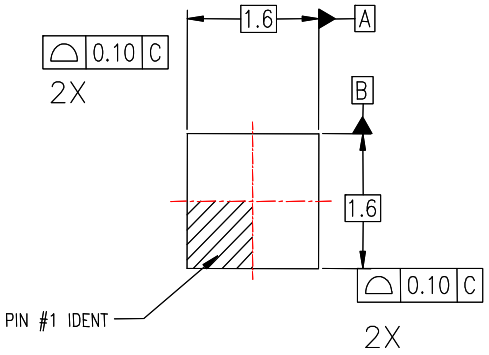
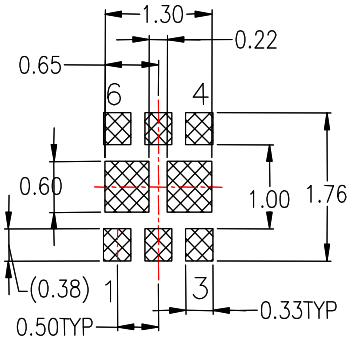



**Figure 14. Junction-to-Ambient Transient Thermal Response Curve**

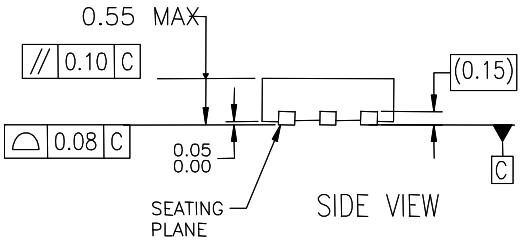
## Dimensional Outline and Pad Layout



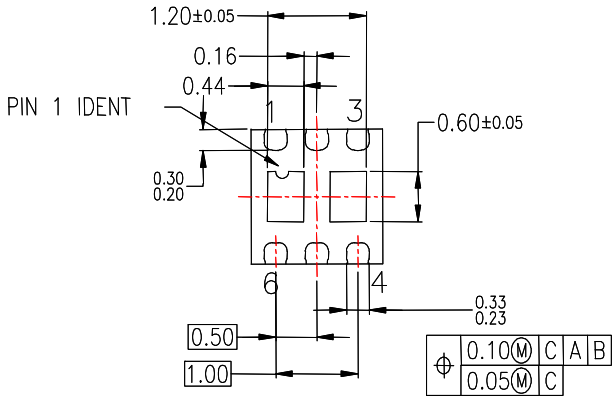

TOP VIEW




RECOMMENDED LAND PATTERN




SIDE VIEW




BOTTOM VIEW

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