

Silicon PNP Power Transistors

2SB722

DESCRIPTION

- With TO-3 package
- High current capability
- High power dissipation

APPLICATIONS

- For power amplifier applications

PINNING(see Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

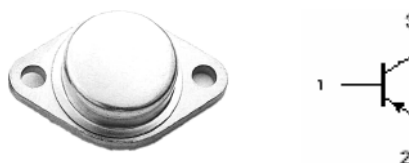


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings($T_a = \square$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	-160	V
V_{CEO}	Collector-emitter voltage	Open base	-160	V
V_{EBO}	Emitter-base voltage	Open collector	-5	V
I_C	Collector current		-15	A
I_B	Base current		-4	A
P_C	Collector power dissipation	$T_C = 25\square$	150	W
T_j	Junction temperature		150	\square
T_{stg}	Storage temperature		-55~200	\square

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CHARACTERISTICS

T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{(BR)CEO}	Collector-emitter breakdown voltage	I _C =-25mA ; I _B =0	-160			V
V _{(BR)CBO}	Collector-base breakdown voltage	I _C =-1mA ; I _E =0	-160			V
V _{(BR)EBO}	Emitter-base breakdown voltage	I _E =-1mA ; I _C =0	-5			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =-10A ; I _B =-1A			-3.0	V
V _{BE}	Base-emitter on voltage	I _C =-2A ; V _{CE} =-5V			-1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =-160V ; I _E =0			-0.1	mA
I _{EBO}	Emitter cut-off current	V _{EB} =-5V ; I _C =0			-0.1	mA
h _{FE}	DC current gain	I _C =-1A ; V _{CE} =-5V	50			

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PACKAGE OUTLINE

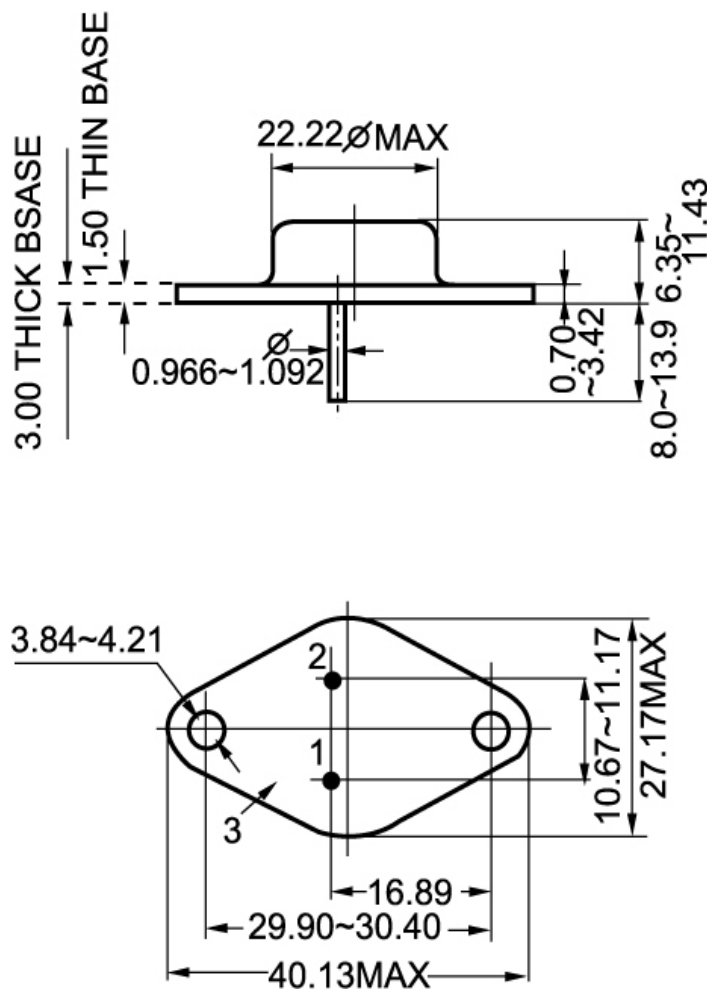


Fig.2 outline dimensions (unindicated tolerance:±0.1mm)