Panasonic

MN3721CFP

4.5mm (1/4 inch) 510H CCD Area Image Sensor

■Overview

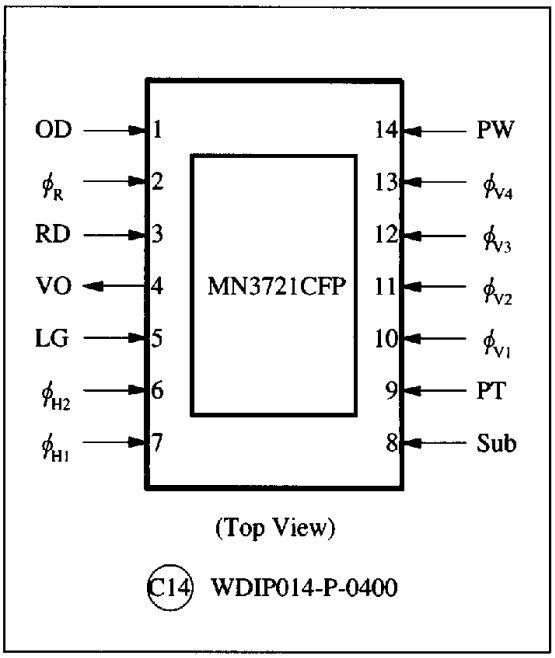
The MN3721CFP is a 4.5mm (1/4 inch) Interline Transfer CCD (IT-CCD) solid state image sensor device.

This device uses photodiodes in the optoelectric conversion section and CCDs for signal read out. The electronic shutter function has made possible an exposure time of 1/10000 seconds. Further, this device has the features of high sensitivity, low noise, broad dynamic range, and low smear.

This device has a total of 320K pixels (542 horizontal×584 vertical) and provides stable and clear images with a resolution of 330 horizontal TV-lines and 420 vertical TV-lines.

Type No.	Size	System	Color or B/W
MN3721CFP	4.5mm (1/4 inch)	P A L	Color

■Pin Assignments



(Top View)

C14 WDIP014-P-0400

■Features

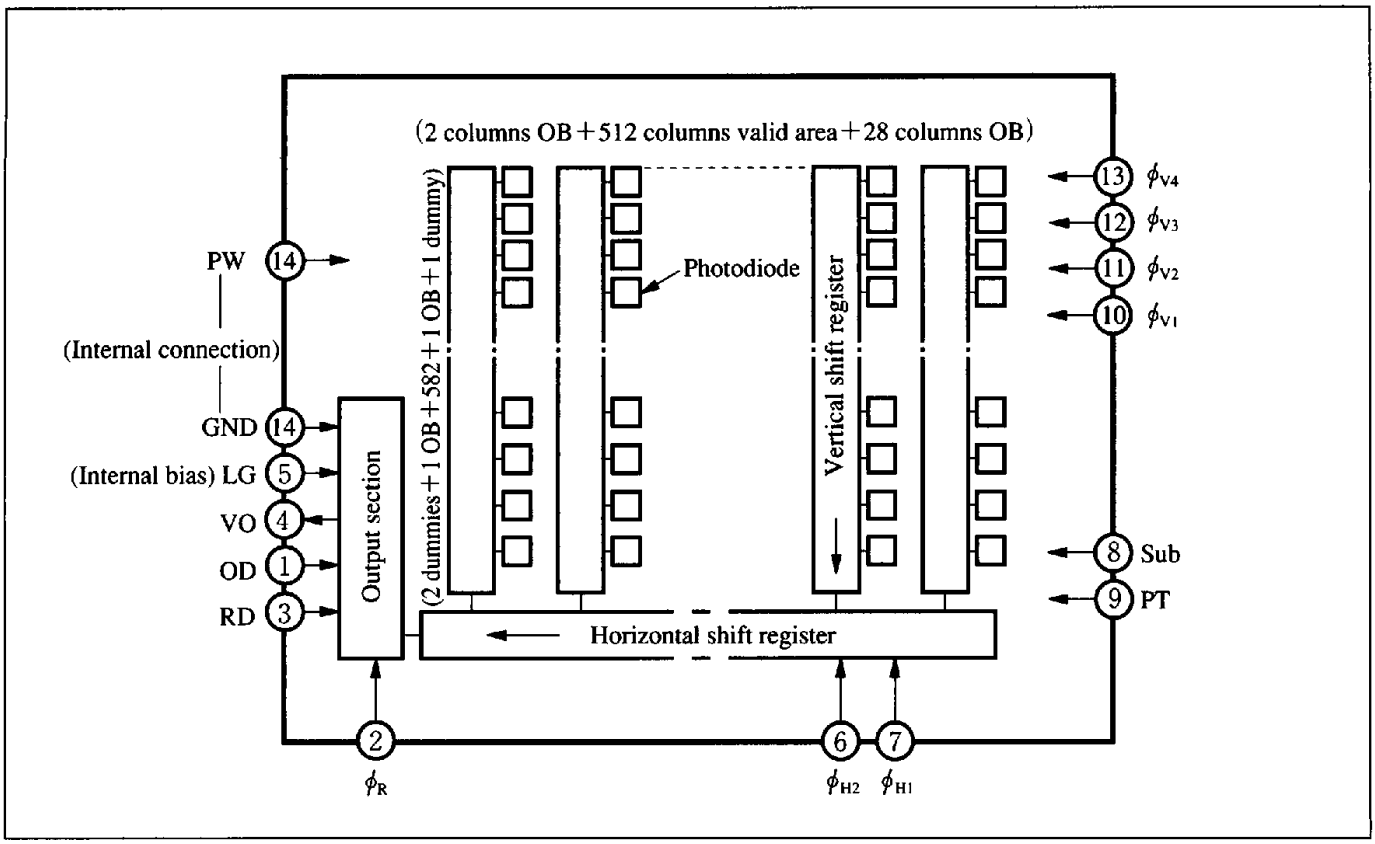
- ●Total number of pixels: 542 (horizontal)×584 (vertical)
- ●High sensitivity
- ●Low noise
- ●Broad dynamic range
- ●Low smear
- ●Low image lag
- ●Electronic shutter function present
- ●No image distortion
- ●Small size enables design of compact equipment
- ●High reliability
- ●14 Pin DIL ceramic package

■Applications

- ●Compact lightweight camcoders
- ●Cameras for surveillance, measurement, and medical use

Area Image Sensors

■Block Diagram



■Pin Descriptions

Pin No.	Symbol	Descriptions	Pin No.	Symbol	Descriptions
1	OD	Output drain	8	Sub	Substrate
2	ϕ_R	Reset pulse	9	PT	P-well for protection circuit
3	RD	Reset drain	10	ϕ_{V1}	Vertical shift register clock pulse (1)
4	VO	Video output	11	ϕ_{V2}	Vertical shift register clock pulse (2)
5	LG	Output load transistor gate	12	ϕ_{V3}	Vertical shift register clock pulse (3)
6	ϕ_{H2}	Horizontal register clock pulse (2)	13	ϕ_{V4}	Vertical shift register clock pulse (4)
7	ϕ_{H1}	Horizontal register clock pulse (1)	14	PW	P-well

■Absolute Maximum Ratings and Operating Conditions

Parameter	Symbol	Rating Note 2)		Operating condition Note 1)			Unit
		min	max	min	typ	max	
Reset drain voltage	V_{RD}	−0.2	18	14.5	15.0	15.5	V
Output drain voltage	V_{OD}	−0.2	18	14.5	15.0	15.5	V
Output load transistor gate voltage Note 3)	V_{LG}	(Supplied internally)					V
Protection P well voltage	V_{PT}	−10.0	0.2	$\phi_{V(L)}$ −1.2	$\phi_{V(L)}$ −1.0	$\phi_{V(L)}$ −0.7	V
P well voltage	V_{PW}	Reference voltage		—	0	—	V
Reset pulse voltage H-L	$V_{\phi R\ (H-L)}$ *1	—	18	4.7	5.0	5.3	V
Reset pulse voltage Bias	$V_{\phi R\ (Bias)}$ *1	−0.2	—	0	Adjust	5.0	V
Horizontal register clock pulse voltage 1	$V_{\phi H1\ (H)}$	—	18	4.7	5.0	5.3	V
	$V_{\phi H1\ (L)}$	−0.2	—	0	0	0	V
Horizontal register clock pulse voltage 2	$V_{\phi H2\ (H)}$	—	18	4.7	5.0	5.3	V
	$V_{\phi H2\ (L)}$	−0.2	—	0	0	0	V
Vertical shift register clock pulse voltage 1	$V_{\phi V1\ (H)}$	—	18	14.5	15.0	15.5	V
	$V_{\phi V1\ (M)}$	—	—	−0.2	0	0.2	V
	$V_{\phi V1\ (L)}$	−9	—	−7.3	−7.0	−6.7	V
Vertical shift register clock pulse voltage 2	$V_{\phi V2\ (M)}$	—	15	0.8	1.0	1.2	V
	$V_{\phi V2\ (L)}$	−9	—	−7.3	−7.0	−6.7	V
Vertical shift register clock pulse voltage 3	$V_{\phi V3\ (H)}$	—	18	14.5	15.0	15.5	V
	$V_{\phi V3\ (M)}$	—	—	−0.2	0	0.2	V
	$V_{\phi V3\ (L)}$	−9	—	−7.3	−7.0	−6.7	V
Vertical shift register clock pulse voltage 4	$V_{\phi V4\ (M)}$	—	15	0.8	1.0	1.2	V
	$V_{\phi V4\ (L)}$	−9	—	−7.3	−7.0	−6.7	V
Substrate voltage	V_{Sub} *2	−0.2	45	3.0	Adjust	14.5	V
	ϕV_{Sub} *2			24.5	25.0	25.5	V
Operating temperature	T_{opr}	−10	70	—	25.0	—	℃
Storage temperature	T_{stg}	−30	80	—	—	—	℃

Note 1) The initial setting of V_{Sub} shall be 8.0V and shall be adjusted to the minimum voltage at which no blooming is caused at a light input of 100 times the standard value. The standard light input is the one when the exposure is done at an aperture of F/8 using a light source of 2856K and 1050nt, and placing a color temperature conversion filter LB-40 (Hoya) and an IR cutting filter CAW-500 (t=2.5mm) in the light path. (F/1.4 20.5nt)

If any FPN picture is present at the minimum operating condition of V_{Sub}, it should be adjusted to the minimum voltage at which there is no FPN picture.

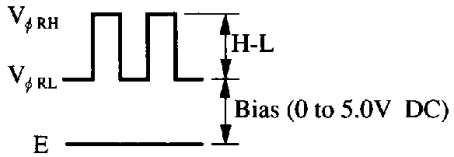
When any overflow charge is present, it should be adjusted to the minimum voltage at which the overflow charge is eliminated in the range under 13.5V.

Note 2) Absolute maximum ratings: $-0.2 < V_{Sub} - V_{PT} < +55$ (V)

$-0.2 < V_{\phi V} - V_{PT} < +24.5$ (V)

Note 3) The LG pin should be grounded via a capacitor of 0.047 μF or more.

*1



*2 V_{Sub} when using electronic shutter function

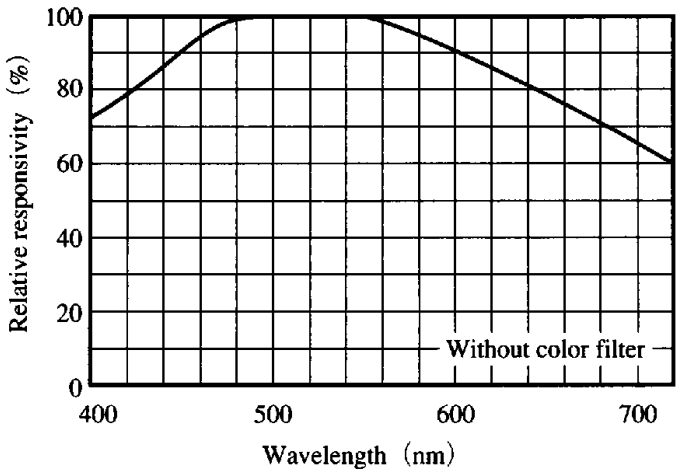
■Optical Characteristics

Type No.	Color or B/W	Valid pixels H	Valid pixels V	S/N typ. (dB)	Saturation output typ. (mV)	Sensitivity F8 typ. (mV)	Vertical smear Sm typ. (%)	Image lag typ. (%)	Horizontal resolution typ. (TV-lines)	Vertical resolution typ. (TV-lines)
MN3721CFP	Color	512	582	58	650	200	0.01	0	330	420

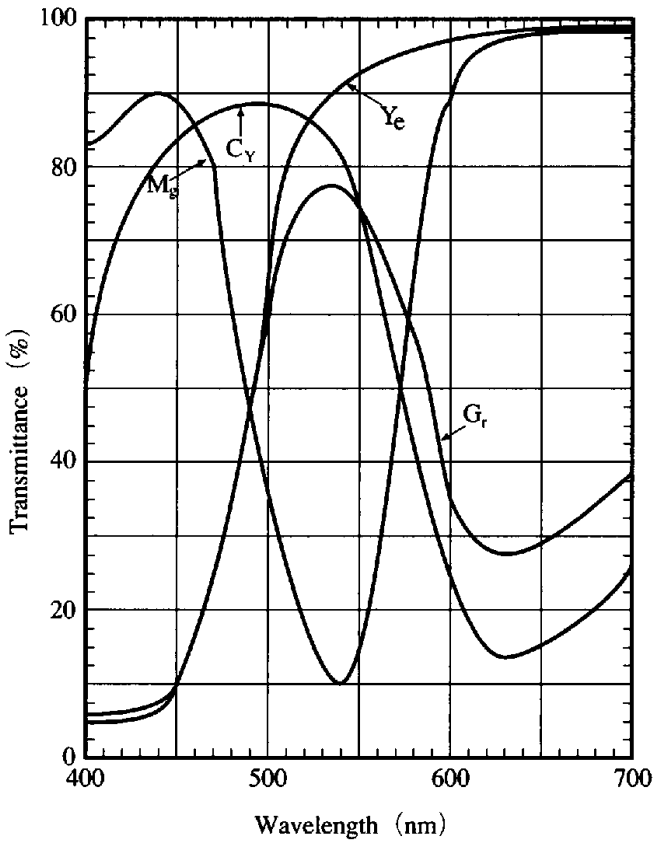
Area Image Sensors

■Graphs of Characteristics

CCD Spectral Characteristics



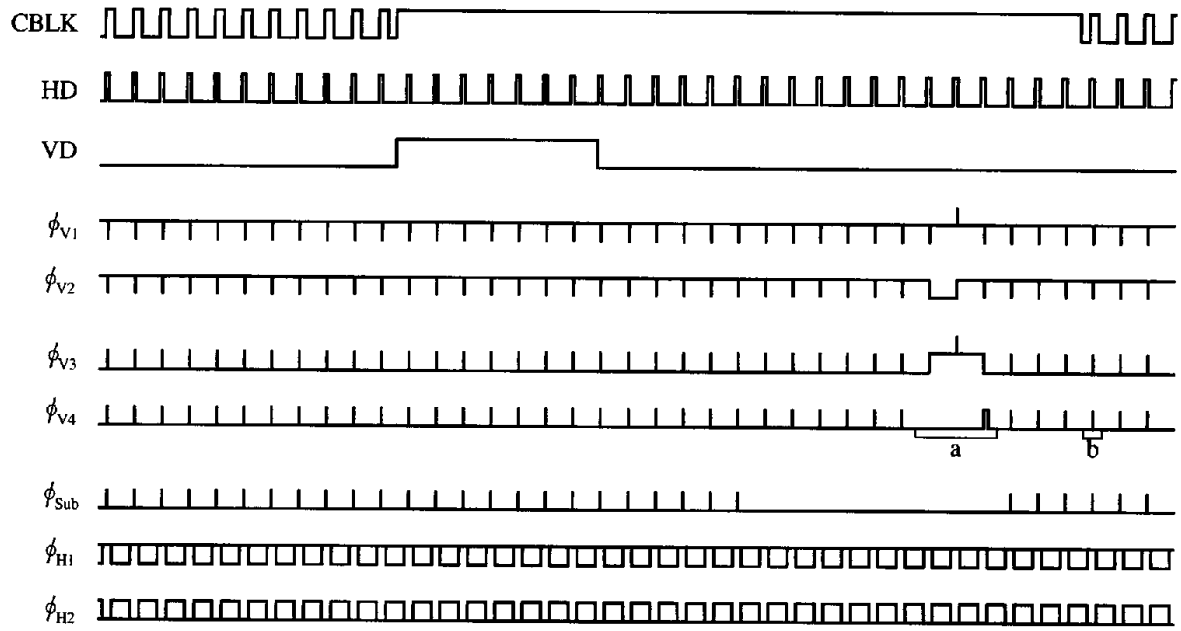
Color Filter Spectral Characteristics



■Example of Recommended Driving Pulses

●V Rate timing

<Field A>



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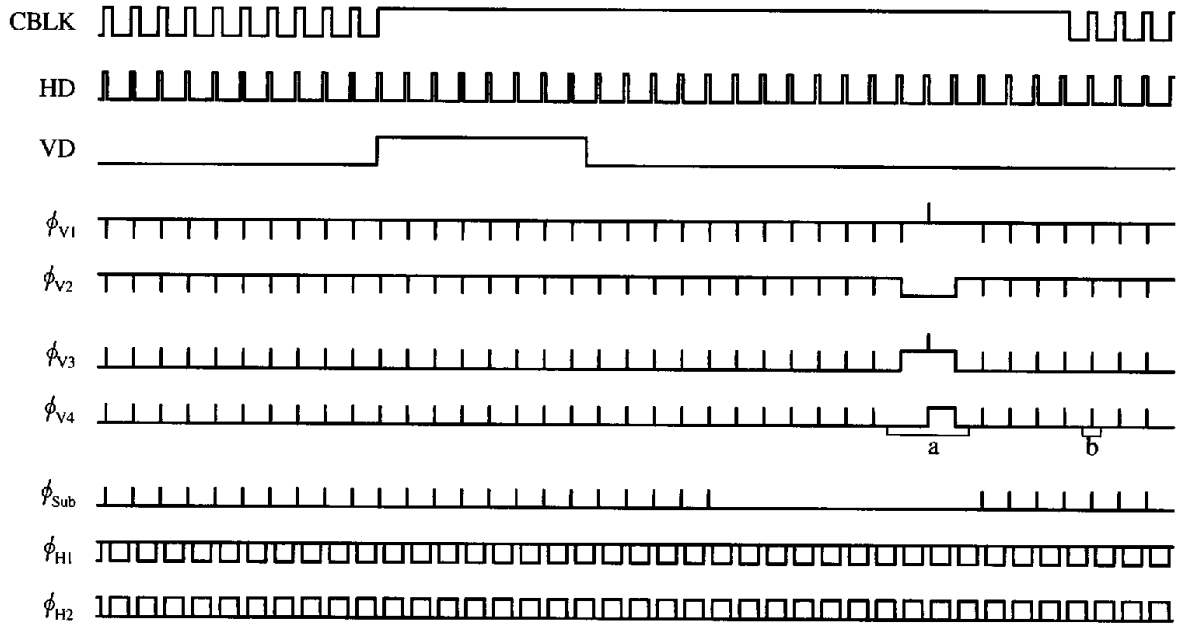
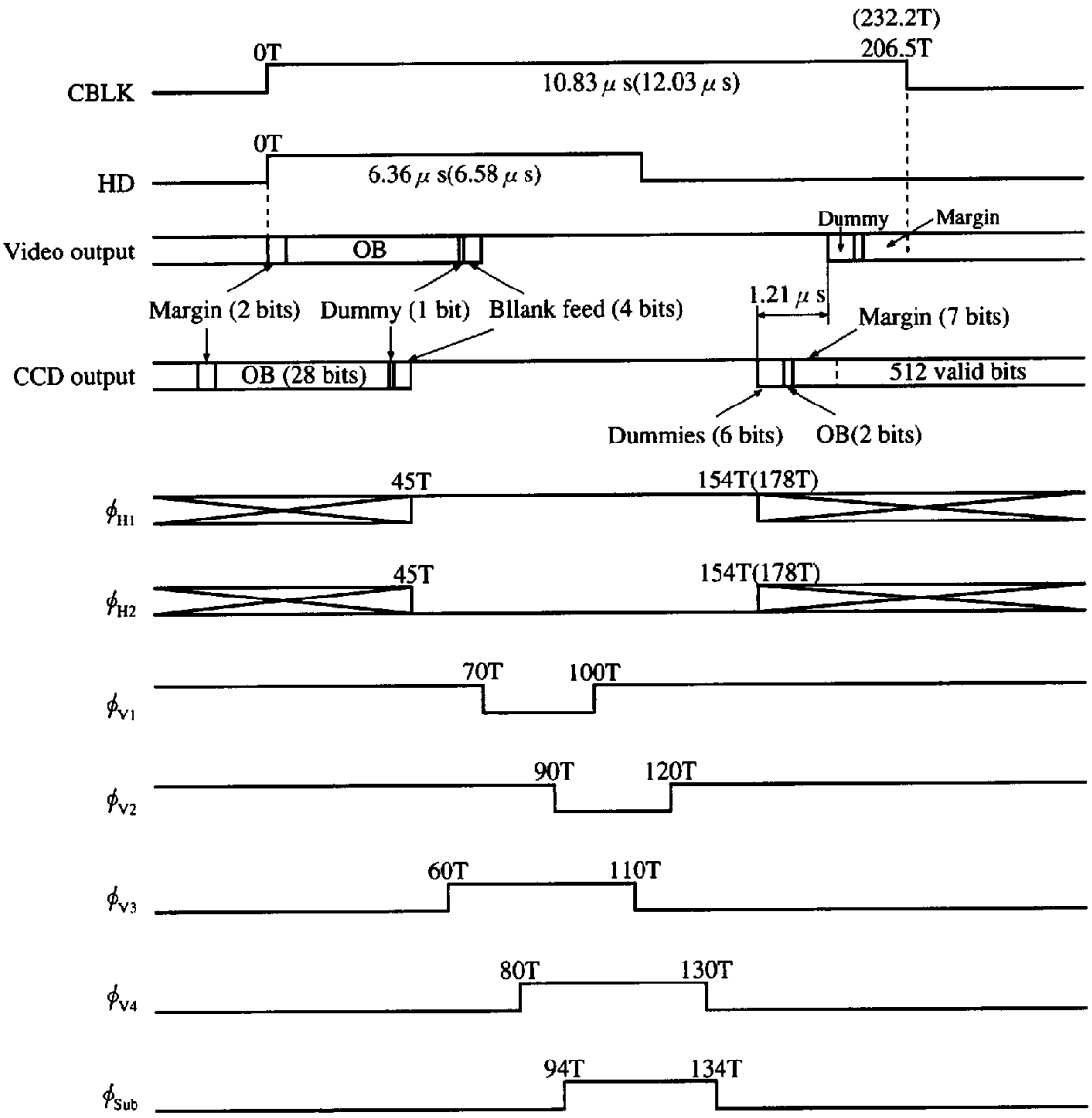


●H Rate timing



●High speed pulse timing