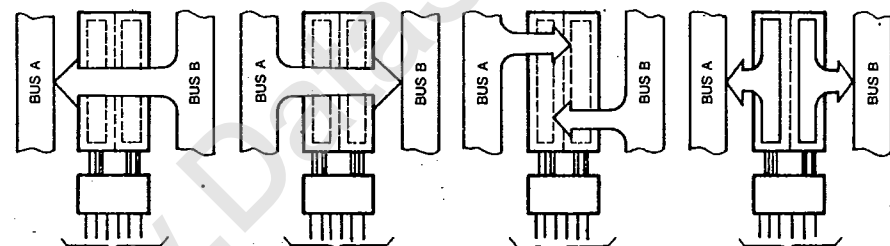
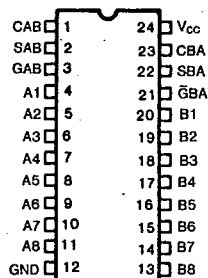


KS54AHCT 651/652
KS74AHCT
Octal 3-State Bus Transceivers
with Registers

T-52-31

Preliminary Specifications
FEATURES

- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored-Data
- Choice of Time and Inverting Data Paths
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- 3-State outputs with high drive current ($I_{OL} = 24 \text{ mA}$ @ $V_{OL} = 0.5\text{V}$) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
KS74AHCT: -40°C to $+85^{\circ}\text{C}$
KS54AHCT: -55°C to $+125^{\circ}\text{C}$
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATION


(3)	(21)	(1)	(23)	(2)	(22)	(3)	(21)	(1)	(23)	(2)	(22)	(3)	(21)	(1)	(23)	(2)	(22)	(3)	(21)	(1)	(23)	(2)	(22)
GAB	GBA	CAB	CBA	SAB	SBA	GAB	GBA	CAB	CBA	SAB	SBA	GAB	GBA	CAB	CBA	SAB	SBA	GAB	GBA	CAB	CBA	SAB	SBA
L	L	X	X	X	L	L	H	X	X	X	L	X	X	X	X	X	X	L	L	X	X	X	H
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	H	H	X	X	X	X

 Real-Time transfer
bus B to bus A

 Real-Time transfer
bus A to bus B

 Storage from
A AND/OR B

 Transfer stored data
TO A AND/OR B


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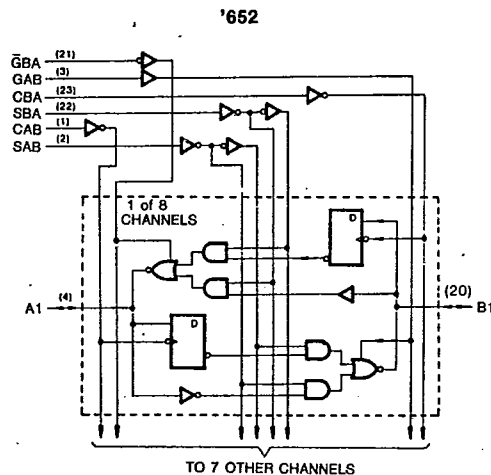
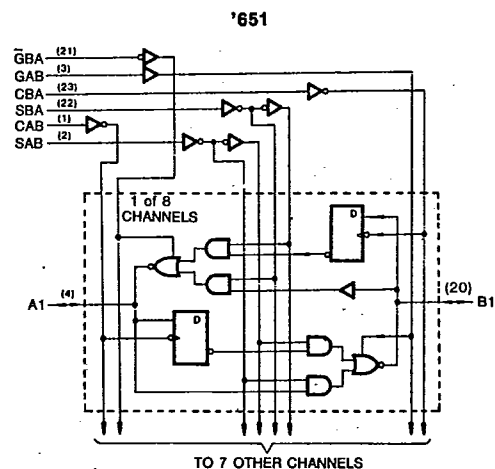
KS54AHCT 651/652
KS74AHCT
Octal 3-State Bus Transceivers
with Registers
FUNCTION TABLE

INPUTS				DATA I/O*		OPERATION OR FUNCTION	
GAB $\bar{G}BA$	CAB	CBA	SAB SBA	A1 THRU A8	B1 THRU B8	'651	'652
L H	H or L	H or L	X ^{ro} X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
L H	↑	↑	X X	Input	Input	Store A, Hold B	Store A Hold B
X H	↑	H or L	X X	Input	Not specified	Store A in both registers	Store A in both registers
H H	↑	↑	X** X	Input	Output*		
L X	H or L	↑	X X	Not specified	Input	Hold A, Store B	Hold A, Store B
L L	↑	↑	X X*	Output*	Input	Store B in both registers	Store B in both registers
L L	X	X	X L	Output	Input	Real-Time \bar{B} Data to A Bus Stored \bar{B} Data to A Bus	Real-Time B Data to a Bus Stored B Data to A Bus
H H	X	X	L X	Input	Output	Real-Time \bar{A} Data to B Bus Stored \bar{A} Data to Bus	Real-Time A Data to B Bus Stored A Data to B Bus
H H	H or L	X	H X				
H L	H or L	H or L	H H	Output	Output	Stored \bar{A} Data to B Bus and Stored \bar{B} Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

* The data output functions may be enabled or disabled by various signals at the GAB and $\bar{G}BA$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

** Select control=L: clocks can occur simultaneously

Select control=H: clocks must be staggered in order to load both registers

LOGIC DIAGRAMS


KS54AHCT 651/652
KS74AHCT**Octal 3-State Bus Transceivers**
with Registers**Absolute Maximum Ratings***

Supply Voltage Range V_{CC} -0.5V to +7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 70 mA
 Continuous Current Through
 V_{CC} or GND pins ± 250 mA
 Storage Temperature Range, T_{stg} ... -85°C to +150°C
 Power Dissipation Per Package, P_d † 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:

Plastic Package (N): -12mW/°C from 65°C to 85°C
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN} , V_{OUT} ... 0V to V_{CC}
 Operating Temperature*

Range KS74AHCT: -40°C to +85°C
 KS54AHCT: -55°C to +125°C

Input Rise & Fall Times, t_r , t_f Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT	KS54AHCT		Unit
			Typ	Guaranteed Limits				
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0		V
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8		V
Minimum High-Level Output Voltage	V _{OH}	V _{IN} =V _{IH} or V _{IL} I _O =-20μA I _O =-6mA	V _{CC} 4.2	V _{CC} - 0.1 3.98	V _{CC} - 0.1 3.84	V _{CC} - 0.1 3.7		V
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20μA I _O =12mA I _O =24mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4		V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0		μA
Maximum 3-State Leakage Current	I _{OZ}	Output Enable =V _{IH} V _{OUT} =V _{CC} or GND		±0.5	±5.0	±10.0		μA
Maximum Quiescent Supply Current	I _{CC}	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0		μA
Additional Worst Case Supply Current	ΔI _{CC}	per input pin V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0		mA



KS54AHCT 651/652
KS74AHCT**Octal 3-State Bus Transceivers
with Registers****AC ELECTRICAL CHARACTERISTICS** (Input $t_r, t_f \leq 2$ ns), AHCT651, AHCT652

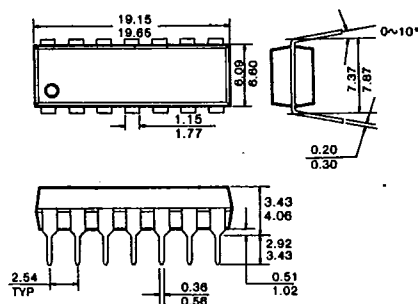
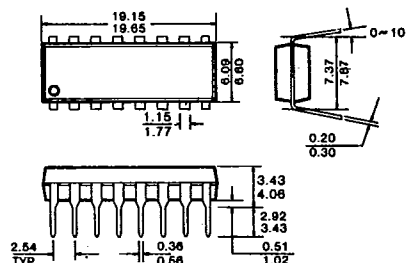
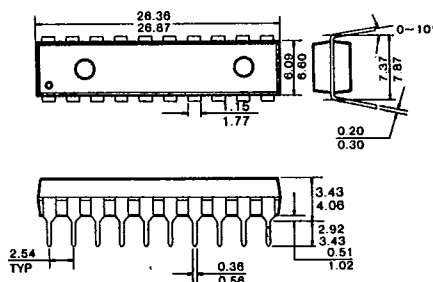
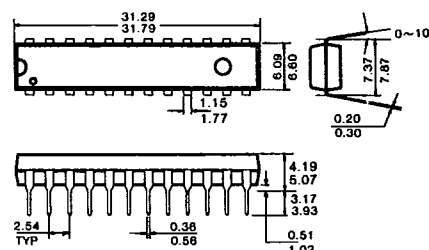
Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Clock Frequency	f_{max}	$C_L = 50\text{pF}$	45	30		25		MHz
Propagation Delay, A or B Input to B or A Output	t_{PLH}	$C_L = 50\text{pF}$	11		18		22	ns
		$C_L = 150\text{pF}$	14		23		28	
	t_{PHL}	$C_L = 50\text{pF}$	11		18		22	ns
		$C_L = 150\text{pF}$	14		23		28	
Propagation Delay, CBA or CAB Input to A or B Output	t_{PLH}	$C_L = 50\text{pF}$	15		25		30	ns
		$C_L = 150\text{pF}$	18		30		36	
	t_{PHL}	$C_L = 50\text{pF}$	15		25		30	ns
		$C_L = 150\text{pF}$	18		30		36	
Propagation Delay, SBA or SAB Input to A or B Output (with A or B High)	t_{PLH}	$C_L = 50\text{pF}$	16		27		32	ns
		$C_L = 150\text{pF}$	19		32		38	
	t_{PHL}	$C_L = 50\text{pF}$	16		27		32	ns
		$C_L = 150\text{pF}$	19		32		38	
Propagation Delay, SBA or SAB Input to A or B Output (with A or B Low)	t_{PLH}	$C_L = 50\text{pF}$	15		25		30	ns
		$C_L = 150\text{pF}$	18		30		36	
Output Enable Time, $\bar{G}BA$ to A or GAB to B	t_{PZL}	$C_L = 50\text{pF}$	19		32		38	ns
		$C_L = 150\text{pF}$	22		37		44	
	t_{PZH}	$R_L = 1\text{k}\Omega$	19		32		38	ns
		$C_L = 150\text{pF}$	22		37		44	
Output Disable Time, $\bar{G}BA$ to A or GAB to B	t_{PHZ}	$R_L = 1\text{k}\Omega$	13		22		26	ns
	t_{PLZ}	$C_L = 50\text{pF}$	13		22		26	
Pulse Width Clocks High or Low	t_w		8	12		15		ns
Setup Time, A before CAB† or B before CBA†	t_{su}		8	12		15		ns
Hold Time, A after CAB† or B after CBA†	t_h		-3	0		0		ns
Maximum Input Capacitance	C_{IN}		5					pF
maximum Output Capacitance	C_{OUT}	Output Disabled	10					pF
Power Dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.



SAMSUNG SEMICONDUCTOR

PACKAGE DIMENSIONS*T-90-20***1. PLASTIC PACKAGES****14-Pin Plastic DIP Units: mm****16-Pin Plastic DIP Units: mm****20-Pin Plastic DIP Units: mm****24-Pin Plastic DIP Units: mm**

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**SAMSUNG SEMICONDUCTOR**

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A-04

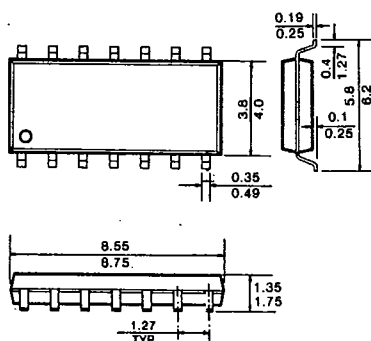
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PACKAGE DIMENSIONS

T-90-20

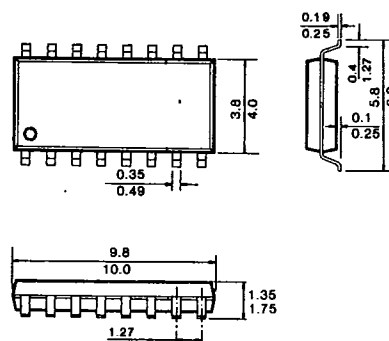
14-Pin SOP

Unit: mm



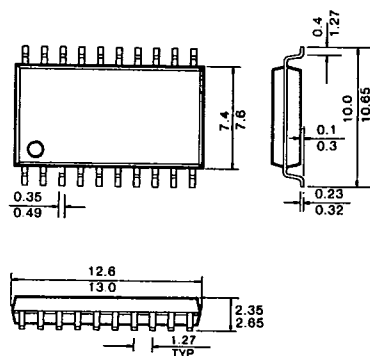
16-Pin SOP

Unit: mm



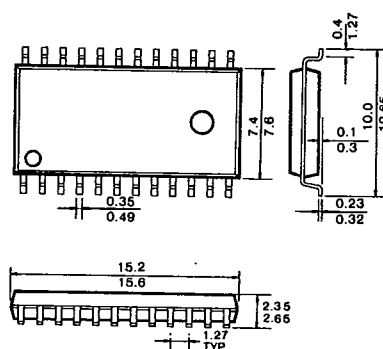
20-Pin SOP

Unit: mm



24-Pin SOP

Unit: mm



SAMSUNG SEMICONDUCTOR

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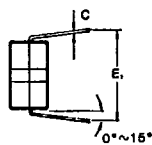
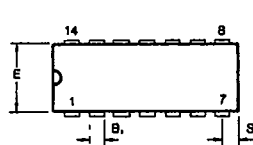
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PACKAGE DIMENSIONS

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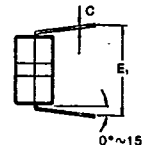
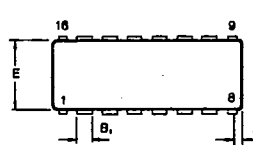
2. CERAMIC PACKAGES

14-Pin Ceramic DIP Units: mm



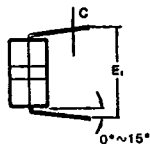
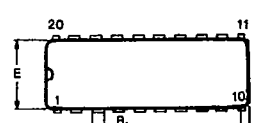
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	8.10	7.49
E ₁	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm



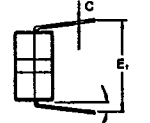
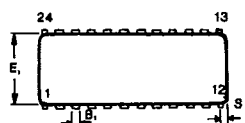
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	8.10	7.49
E ₁	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	25.78	26.93
E	8.10	8.60
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	31.50	32.84
E	7.24	7.75
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.85	1.93



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