

KS54AHCT 845/846

KS74AHCT

8-Bit Bus Interface D-Type Latches with 3-State Outputs

T-46-07-05

Preliminary Specifications

FEATURE

- 3-state buffer-type outputs drive bus-lines directly
- Bus-structured pinout
- Provides extra bus driving latches necessary for wider address/data paths or buses with parity
- Low power consumption characteristic of CMOS devices
- 3-state outputs with high drive current ($I_{OL} = 24\text{mA}$ @ $V_{OL} = 0.5\text{V}$) for direct bus interface
- Direct interface capability with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
KS74AHCT: -40°C to $+85^{\circ}\text{C}$
KS54AHCT: -55°C to 125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

DESCRIPTION

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

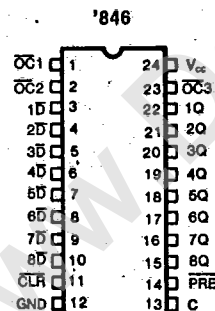
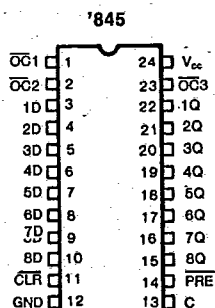
The eight latches are transparent D-type. The '845 has noninverting data(D) inputs. The '846 has inverting D inputs. Since $\overline{\text{CLR}}$ and $\overline{\text{PRE}}$ are independent of the clock, taking the $\overline{\text{CLR}}$ input low will cause the eight Q outputs to go low. Taking the $\overline{\text{PRE}}$ input low will cause the eight Q outputs to go high. When both $\overline{\text{PRE}}$ and $\overline{\text{CLR}}$ are taken low, the outputs will follow the preset condition.

The buffered output control inputs ($\overline{\text{OC1}}$, $\overline{\text{OC2}}$, and $\overline{\text{OC3}}$) can be used to place the eight outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

PIN CONFIGURATIONS



KS54AHCT 845/846
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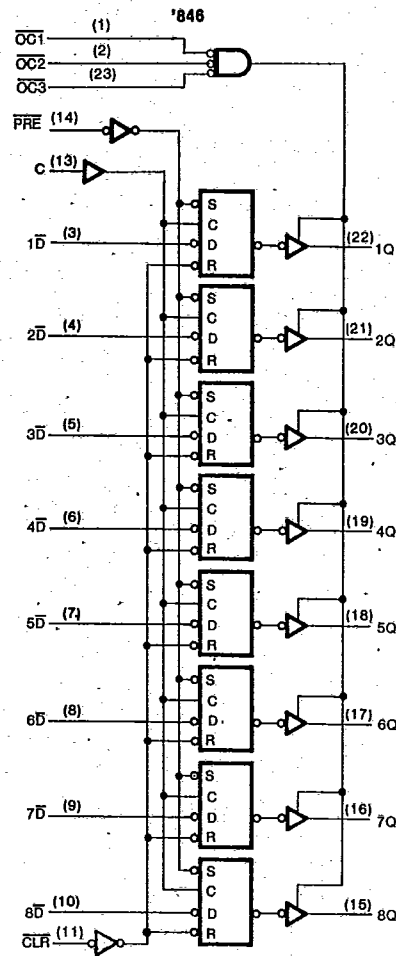
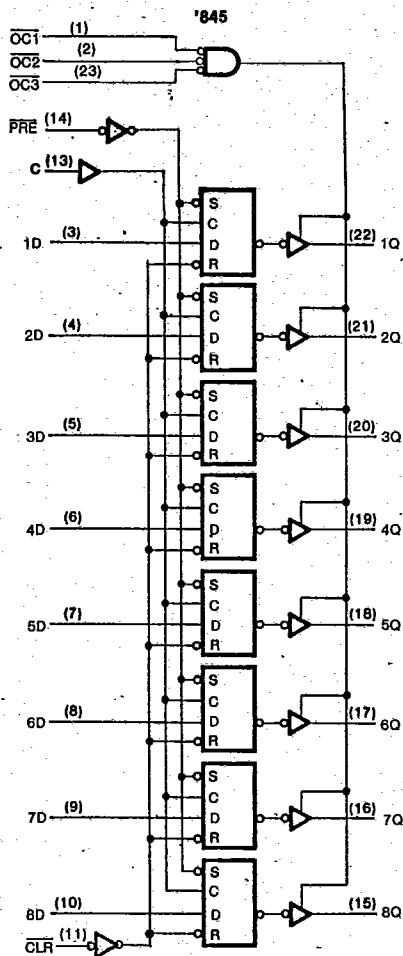
T-46-07-05

FUNCTION TABLE

'845								OUTPUT
INPUTS							Q	
PRE	CLR	OC1	OC2	OC3	C	D		
L	H	L	L	L	X	X	H	
H	L	L	L	L	X	X	L	
L	L	L	L	L	X	X	H	
H	H	L	L	L	H	L	L	
H	H	L	L	L	H	H	H	
H	H	L	L	L	L	X	Q ₀	
X	X	X	X	H	X	X	Z	
X	X	X	H	X	X	X	Z	
X	X	H	X	X	X	X	Z	

'846							OUTPUT
INPUTS							Q
PRE	CLR	OC1	OC2	OC3	C	D	Q
L	H	L	L	L	X	X	H
H	L	L	L	L	X	X	L
L	L	L	L	L	X	X	H
H	H	L	L	L	H	L	H
H	H	L	L	L	H	H	L
H	H	L	L	L	L	X	Q ₀
X	X	X	X	H	X	X	Z
X	X	X	H	X	X	X	Z
X	X	H	X	X	X	X	Z

LOGIC DIAGRAMS



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KS74AHCT
8-Bit Bus Interface D-Type
Latches with 3-State Outputs

T-46-07-05

Absolute Maximum Ratings*

Supply Voltage Range V_{CC} -0.5V to +7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 70 mA
 Continuous Current Through
 V_{CC} or GND pins ± 250 mA
 Storage Temperature Range, T_{stg} ... -65°C to +150°C
 Power Dissipation Per Package, P_d † 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
 Plastic Package (N): -12mW/°C from 65°C to 85°C
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN} , V_{OUT} ... 0V to V_{CC}
 Operating Temperature
 Range

KS74AHCT: -40°C to +85°C
 KS54AHCT: -55°C to +125°C
 Input Rise & Fall Times, t_r , t_f Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T _a = 25°C		KS74AHCT	KS54AHCT	Unit
					T _a = -40°C to +85°C	T _a = -55°C to +125°C	
			Typ	Guaranteed Limits			
Minimum High-Level Input Voltage	V _{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V _{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage	V _{OH}	V _{IN} =V _{IH} or V _{IL} I _O =-20μA I _O =-4mA	V _{CC} 4.2	V _{CC} -0.1 3.98	V _{CC} -0.1 3.84	V _{CC} -0.1 3.7	V
Maximum Low-Level Output Voltage	V _{OL}	V _{IN} =V _{IH} or V _{IL} I _O =20μA I _O =4mA I _O =8mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I _{IN}	V _{IN} =V _{CC} or GND		±0.1	±1.0	±1.0	μA
Maximum Quiescent Supply Current	I _{CC}	V _{IN} =V _{CC} or GND I _{OUT} =0μA		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI _{CC}	per input in V _I =2.4V other Inputs: at V _{CC} or GND I _{OUT} =0μA		2.7	2.9	3.0	mA

KS54AHCT
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T-46-07-05

AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2$ ns), AHCT845

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay Clk to Q	t_{PLH}		13†		22		26	ns
	t_{PHL}		13		22		26	
Propagation Delay D to Q	t_{PLH}		8		15		20	ns
	t_{PHL}		8		15		20	
Propagation Delay CLR to Q	t_{PLH}		16		26		31	ns
	t_{PHL}		16		26		31	
Propagation Delay PRE to Q	t_{PLH}		16		26		31	ns
	t_{PHL}		16		26		31	
Propagation Delay OC to Q	t_{PZH}		12		20		24	ns
	t_{PZL}		12		20		24	
Propagation Delay OC to Q	t_{PHZ}		12		20		24	ns
	t_{PLZ}		12		20		24	
Input Capacitance	C_{IN}		5					pF
Power dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

AC ELECTRICAL CHARACTERISTICS (Input $t_r, t_f \leq 2$ ns), AHCT846

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$	KS74AHCT $T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		KS54AHCT $T_a = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$		Unit
			Typ	Min	Max	Min	Max	
Propagation Delay Clk to Q	t_{PLH}		14		24		32	ns
	t_{PHL}		14		24		32	
Propagation Delay D to Q	t_{PLH}		10		17		22	ns
	t_{PHL}		10		17		22	
Propagation Delay CLR to Q	t_{PLH}		13		22		26	ns
	t_{PHL}		13		22		26	
Propagation Delay PRE to Q	t_{PLH}		13		22		26	ns
	t_{PHL}		13		22		26	
Propagation Delay OC to Q	t_{PZH}		12		20		24	ns
	t_{PZL}		12		20		24	
Propagation Delay OC to Q	t_{PHZ}		12		20		24	ns
	t_{PLZ}		12		20		24	
Input Capacitance	C_{IN}		5					pF
Power dissipation Capacitance*	C_{PD}							pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

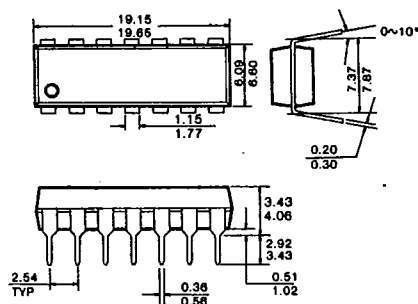
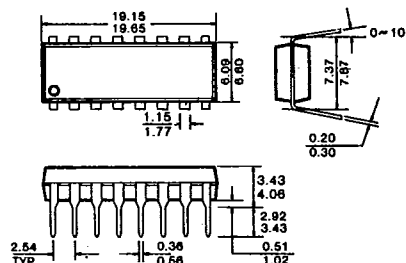
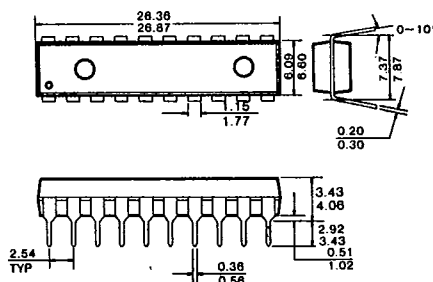
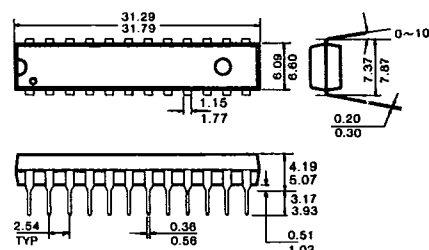
† For AC switching test circuits and timing waveforms see section 2.



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PACKAGE DIMENSIONS

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1. PLASTIC PACKAGES**14-Pin Plastic DIP Units: mm****16-Pin Plastic DIP Units: mm****20-Pin Plastic DIP Units: mm****24-Pin Plastic DIP Units: mm**

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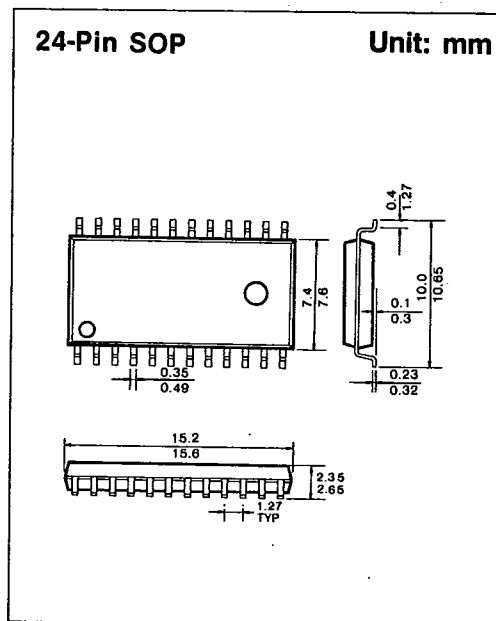
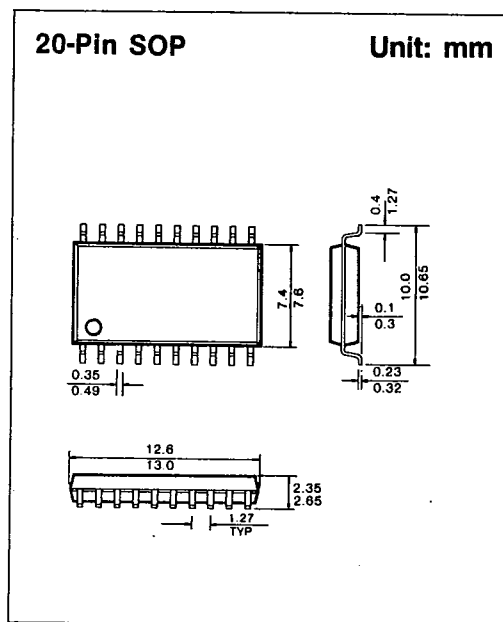
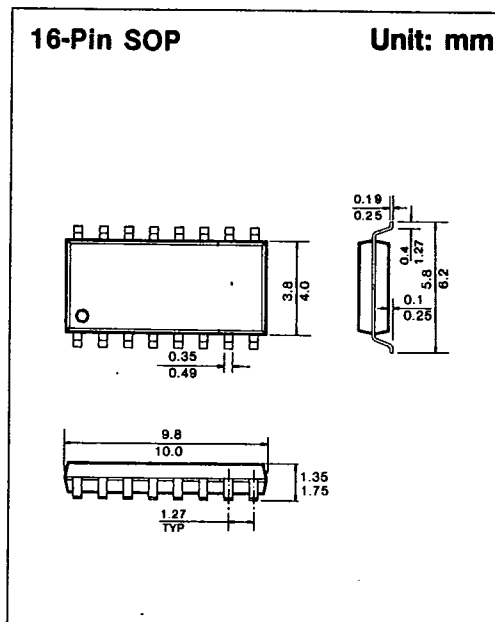
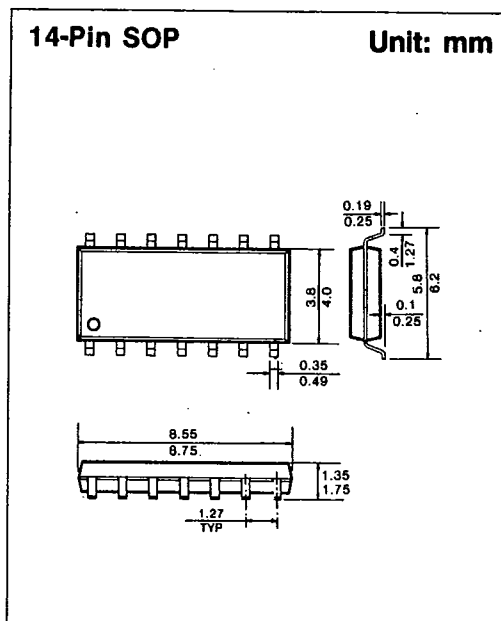
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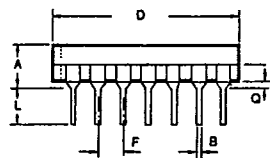
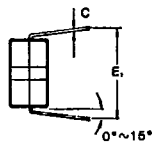
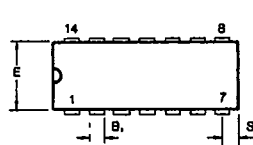
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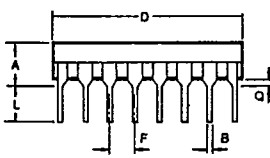
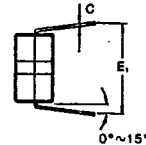
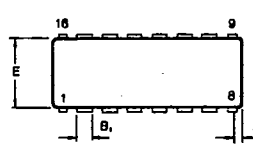


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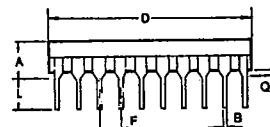
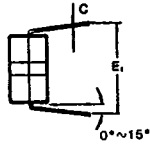
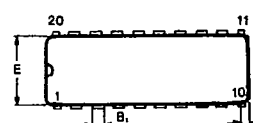
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2. CERAMIC PACKAGES**14-Pin Ceramic DIP Units: mm**

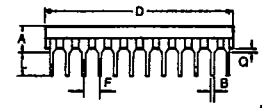
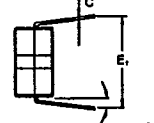
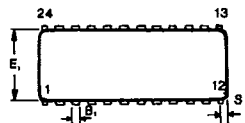
Dim	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	8.10	7.49
E ₁	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B ₁	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	8.10	7.49
E ₁	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	25.78	26.93
E	8.10	8.60
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm

Dim	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B ₁	1.14	1.52
C	0.20	0.38
D	31.50	32.84
E	7.24	7.75
E ₁	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.85	1.93

7



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1677

A-06

783