

DRAM MODULE

KMM372V320(8)0CK4

KMM372V320(8)0CK4 Fast Page Mode

32M x 72 DRAM DIMM with ECC Using 16Mx4, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372V320(8)0C is a 32Mx72bits Dynamic RAM high density memory module. The Samsung KMM372V320(8)0C consists of thirty-six CMOS 16Mx4bits DRAMs in SOJ 400mil packages and two 16 bits driver IC in TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372V320(8)0C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

| Speed | t _{TRAC} | t _{CAC} | t _{RC} | t _{PC} |
|-------|-------------------|------------------|-----------------|-----------------|
| -5 | 50ns | 18ns | 90ns | 35ns |
| -6 | 60ns | 20ns | 110ns | 40ns |

FEATURES

- Part Identification

| Part number | PKG | Ref. | CBR Ref. | ROR Ref. |
|----------------|-----|------|----------|----------|
| KMM372V3200CK4 | SOJ | 4K | 4K/64ms | |
| KMM372V3280CK4 | SOJ | 8K | 4K/64ms | 8K/64ms |

- Fast Page Mode Operation
- CAS-before-RAS Refresh capability
- RAS-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except RAS and DQ
- PCB : Height(2000mil), double sided component

PIN CONFIGURATIONS

| Pin | Front | Pin | Front | Pin | Front | Pin | Back | Pin | Back | Pin | Back |
|-----|-------|-----|-------|-----|-------|-----|------|-----|-------|-----|------|
| 1 | Vss | 29 | *CAS2 | 57 | DQ22 | 85 | Vss | 113 | *CAS3 | 141 | DQ58 |
| 2 | DQ0 | 30 | RAS0 | 58 | DQ23 | 86 | DQ36 | 114 | RAS1 | 142 | DQ59 |
| 3 | DQ1 | 31 | OE0 | 59 | Vcc | 87 | DQ37 | 115 | RFU | 143 | Vcc |
| 4 | DQ2 | 32 | Vss | 60 | DQ24 | 88 | DQ38 | 116 | Vss | 144 | DQ60 |
| 5 | DQ3 | 33 | A0 | 61 | RFU | 89 | DQ39 | 117 | A1 | 145 | RFU |
| 6 | Vcc | 34 | A2 | 62 | RFU | 90 | Vcc | 118 | A3 | 146 | RFU |
| 7 | DQ4 | 35 | A4 | 63 | RFU | 91 | DQ40 | 119 | A5 | 147 | RFU |
| 8 | DQ5 | 36 | A6 | 64 | RFU | 92 | DQ41 | 120 | A7 | 148 | RFU |
| 9 | DQ6 | 37 | A8 | 65 | DQ25 | 93 | DQ42 | 121 | A9 | 149 | DQ61 |
| 10 | DQ7 | 38 | A10 | 66 | DQ26 | 94 | DQ43 | 122 | A11 | 150 | DQ62 |
| 11 | DQ8 | 39 | A12 | 67 | DQ27 | 95 | DQ44 | 123 | *A13 | 151 | DQ63 |
| 12 | Vss | 40 | Vcc | 68 | Vss | 96 | Vss | 124 | Vcc | 152 | Vss |
| 13 | DQ9 | 41 | RFU | 69 | DQ28 | 97 | DQ45 | 125 | RFU | 153 | DQ64 |
| 14 | DQ10 | 42 | RFU | 70 | DQ29 | 98 | DQ46 | 126 | B0 | 154 | DQ65 |
| 15 | DQ11 | 43 | Vss | 71 | DQ30 | 99 | DQ47 | 127 | Vss | 155 | DQ66 |
| 16 | DQ12 | 44 | OE2 | 72 | DQ31 | 100 | DQ48 | 128 | RFU | 156 | DQ67 |
| 17 | DQ13 | 45 | RAS2 | 73 | Vcc | 101 | DQ49 | 129 | RAS3 | 157 | Vcc |
| 18 | Vcc | 46 | CAS4 | 74 | DQ32 | 102 | Vcc | 130 | CAS5 | 158 | DQ68 |
| 19 | DQ14 | 47 | *CAS6 | 75 | DQ33 | 103 | DQ50 | 131 | *CAS7 | 159 | DQ69 |
| 20 | DQ15 | 48 | W2 | 76 | DQ34 | 104 | DQ51 | 132 | PDE | 160 | DQ70 |
| 21 | DQ16 | 49 | Vcc | 77 | DQ35 | 105 | DQ52 | 133 | Vcc | 161 | DQ71 |
| 22 | DQ17 | 50 | RSVD | 78 | Vss | 106 | DQ53 | 134 | RSVD | 162 | Vss |
| 23 | Vss | 51 | RSVD | 79 | PD1 | 107 | Vss | 135 | RSVD | 163 | PD2 |
| 24 | RSVD | 52 | DQ18 | 80 | PD3 | 108 | RSVD | 136 | DQ54 | 164 | PD4 |
| 25 | RSVD | 53 | DQ19 | 81 | PD5 | 109 | RSVD | 137 | DQ55 | 165 | PD6 |
| 26 | Vcc | 54 | Vss | 82 | PD7 | 110 | Vcc | 138 | Vss | 166 | PD8 |
| 27 | W0 | 55 | DQ20 | 83 | ID0 | 111 | RFU | 139 | DQ56 | 167 | ID1 |
| 28 | CAS0 | 56 | DQ21 | 84 | Vcc | 112 | CAS1 | 140 | DQ57 | 168 | Vcc |

NOTE : A12 is used for only KMM372V3280CK4 (8K Ref.)

PD Note : PD & ID Terminals must each be pulled up through a register to Vcc at the next higher level assembly. PDs will be either open (NC) or driven to Vss via on-board buffer circuits.
ID Note : IDs will be either open (NC) or connected directly to Vss without a buffer.

PIN NAMES

| Pin Names | Function |
|------------------|-------------------------|
| A0, B0, A1 - A11 | Address Input(4K ref) |
| A0, B0, A1 - A12 | Address Input(8K ref) |
| DQ0 - DQ71 | Data In/Out |
| W0, W2 | Read/Write Enable |
| OE0, OE2 | Output Enable |
| RAS0 - RAS3 | Row Address Strobe |
| CAS0, 1,4,5 | Column Address Strobe |
| Vcc | Power(+3.3V) |
| Vss | Ground |
| NC | No Connection |
| PDE | Presence Detect Enable |
| PD1 - 8 | Presence Detect |
| ID0 - 1 | ID bit |
| RSVD | Reserved Use |
| RFU | Reserved for Future Use |

Pins marked '*' are not used in this module.

PD & ID Table

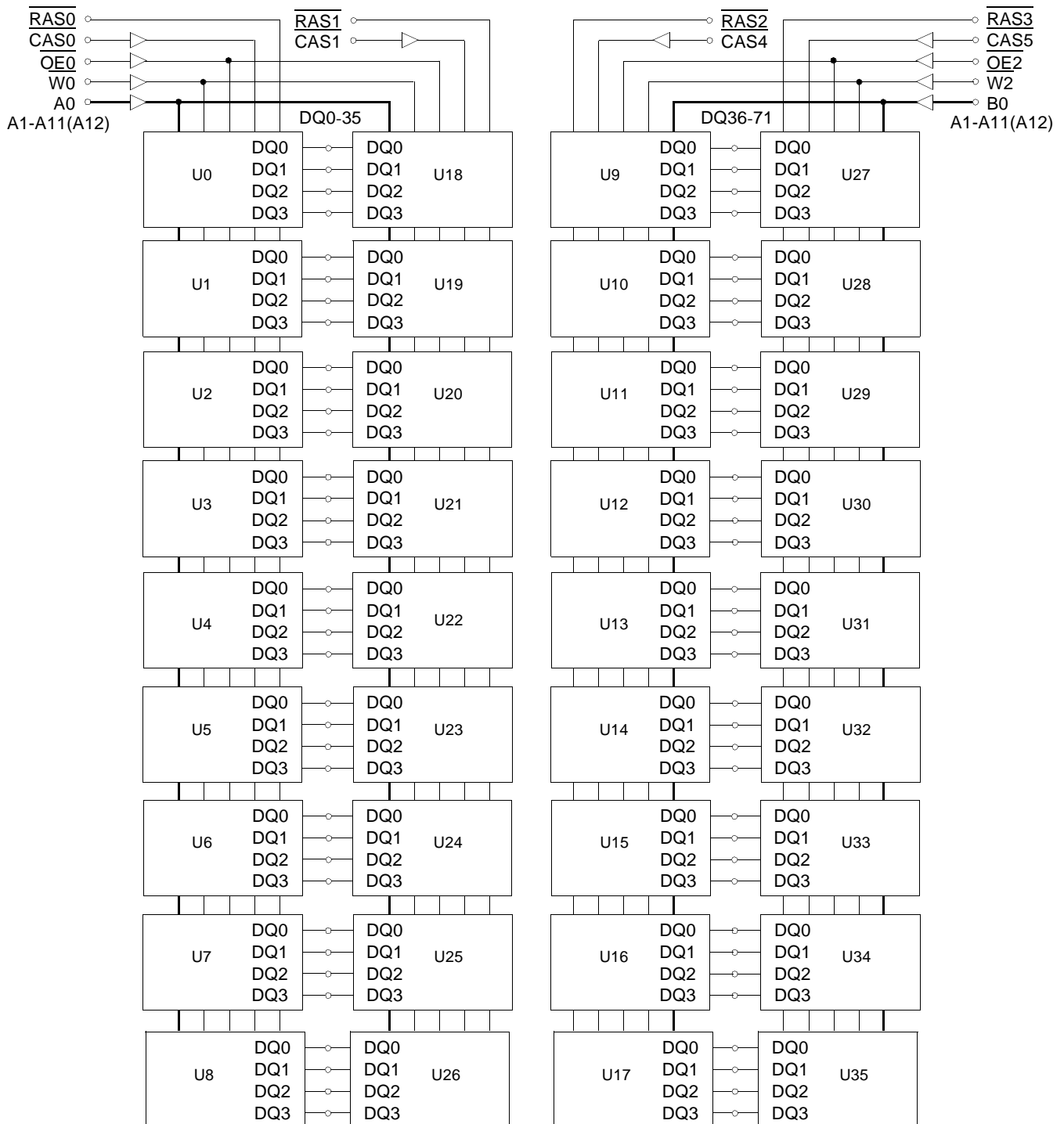
| Pin | 50NS | 60NS |
|-----|------|------|
| PD1 | 1 | 1 |
| PD2 | 0 | 0 |
| PD3 | 0 | 0 |
| PD4 | 0 | 0 |
| PD5 | 0 | 0 |
| PD6 | 0 | 1 |
| PD7 | 0 | 1 |
| PD8 | 0 | 0 |
| ID0 | 0 | 0 |
| ID1 | 0 | 0 |

PD : 0 for Vol of Drive IC & 1 for N.C
ID : 0 for Vss & 1 for N.C

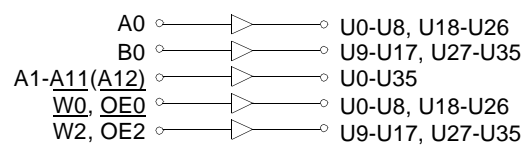
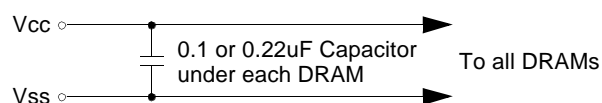
DRAM MODULE

KMM372V320(8)0CK4

FUNCTIONAL BLOCK DIAGRAM



NOTE : A12 is used for only KMM372V3280CK4(8K Ref.)



ABSOLUTE MAXIMUM RATINGS *

| Item | Symbol | Rating | Unit |
|---------------------------------------|------------------------------------|--------------|------|
| Voltage on any pin relative Vss | V _{IN} , V _{OUT} | -0.5 to +4.6 | V |
| Voltage on Vcc supply relative to Vss | V _{CC} | -0.5 to +4.6 | V |
| Storage Temperature | T _{stg} | -55 to +125 | °C |
| Power Dissipation | P _D | 36 | W |
| Short Circuit Output Current | I _{OS} | 50 | mA |

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to Vss, TA = 0 to 70°C)

| Item | Symbol | Min | Typ | Max | Unit |
|--------------------|-----------------|--------------------|-----|------------------------------------|------|
| Supply Voltage | V _{CC} | 3.0 | 3.3 | 3.6 | V |
| Ground | V _{SS} | 0 | 0 | 0 | V |
| Input High Voltage | V _{IH} | 2.0 | - | V _{CC} +0.3 ^{*1} | V |
| Input Low Voltage | V _{IL} | -0.3 ^{*2} | - | 0.8 | V |

*1 : V_{CC}+1.3V at pulse width≤15ns, which is measured at V_{CC}.

*2 : -1.3V at pulse width≤15ns, which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

| Symbol | Speedl | KMM372V3200CK4 | | KMM372V3280CK4 | | Unit |
|-------------------|------------|----------------|------|----------------|------|------|
| | | Min | Max | Min | Max | |
| I _{CC1} | -5 | - | 1998 | - | 1458 | mA |
| | -6 | - | 1818 | - | 1278 | mA |
| I _{CC2} | Don't care | - | 100 | - | 100 | mA |
| I _{CC3} | -5 | - | 1998 | - | 1458 | mA |
| | -6 | - | 1818 | - | 1278 | mA |
| I _{CC4} | -5 | - | 1098 | - | 1098 | mA |
| | -6 | - | 918 | - | 918 | mA |
| I _{CC5} | Don't care | - | 30 | - | 30 | mA |
| I _{CC6} | -5 | - | 1998 | - | 1998 | mA |
| | -6 | - | 1818 | - | 1818 | mA |
| I _{I(L)} | Don't care | -10 | 10 | -10 | 10 | uA |
| I _{O(L)} | | -10 | 10 | -10 | 10 | uA |
| V _{OH} | Don't care | 2.4 | - | 2.4 | - | V |
| V _{OL} | | - | 0.4 | - | 0.4 | V |

I_{CC1}* : Operating Current * ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address cycling @trc=min)

I_{CC2} : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=\text{V}_{\text{IH}}$)

I_{CC3}* : $\overline{\text{RAS}}$ Only Refresh Current * ($\overline{\text{CAS}}=\text{V}_{\text{IH}}$, $\overline{\text{RAS}}$ cycling @trc=min)

I_{CC4}* : Fast Page Mode Current * ($\overline{\text{RAS}}=\text{V}_{\text{IL}}$, $\overline{\text{CAS}}$ cycling : tpc=min)

I_{CC5} : Standby Current ($\overline{\text{RAS}}=\overline{\text{CAS}}=\overline{\text{W}}=\text{V}_{\text{CC}}-0.2\text{V}$)

I_{CC6}* : $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Current * ($\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ cycling @trc=min)

I_{I(L)} : Input Leakage Current (Any input 0 ≤ V_{IN} ≤ V_{CC}+0.3V, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, 0V ≤ V_{OUT} ≤ V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{\text{RAS}}=\text{V}_{\text{IL}}$. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, tpc.

DRAM MODULE

KMM372V320(8)0CK4

CAPACITANCE (TA = 25°C, f = 1MHz)

| Item | Symbol | Min | Max | Unit |
|-------------------------------------|--------|-----|-----|------|
| Input capacitance[A0, B0, A1 - A12] | CIN1 | - | 20 | pF |
| Input capacitance[W0, W2, OE0, OE2] | CIN2 | - | 20 | pF |
| Input capacitance[RAS0 - RAS3] | CIN3 | - | 73 | pF |
| Input capacitance[CAS0, CAS1,4,5] | CIN4 | - | 20 | pF |
| Input/Output capacitance[DQ0 - 71] | CDQ | - | 24 | pF |

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=3.3V±0.3V. See notes 1,2.)

Test condition : Vih/Vil=2.2/0.7V, Voh/Vol=2.0/0.8V, output loading CL=100pF

| Parameter | Symbol | -5 | | -6 | | Unit | Note |
|-------------------------------------|--------|-----|-----|-----|-----|------|----------|
| | | Min | Max | Min | Max | | |
| Random read or write cycle time | tRC | 90 | | 110 | | ns | |
| Read-modify-write cycle time | tRWC | 133 | | 155 | | ns | |
| Access time from RAS | tRAC | | 50 | | 60 | ns | 3,4,10 |
| Access time from CAS | tCAC | | 18 | | 20 | ns | 3,4,5,11 |
| Access time from column address | tAA | | 30 | | 35 | ns | 3,10,11 |
| CAS to output in Low-Z | tCLZ | 5 | | 5 | | ns | 3,11 |
| Output buffer turn-off delay | tOFF | 5 | 18 | 5 | 20 | ns | 6,11 |
| Transition time(rise and fall) | tT | 1 | 50 | 1 | 50 | ns | 2 |
| RAS precharge time | tRP | 30 | | 40 | | ns | |
| RAS pulse width | tRAS | 50 | 10K | 60 | 10K | ns | |
| RAS hold time | tRSH | 18 | | 20 | | ns | 11 |
| CAS hold time | tCSH | 48 | | 58 | | ns | 11 |
| CAS pulse width | tCAS | 13 | 10K | 15 | 10K | ns | |
| RAS to CAS delay time | tRCD | 18 | 32 | 18 | 40 | ns | 4,11 |
| RAS to column address delay time | tRAD | 13 | 20 | 13 | 25 | ns | 10,11 |
| CAS to RAS precharge time | tCRP | 10 | | 10 | | ns | 11 |
| Row address set-up time | tASR | 5 | | 5 | | ns | 11 |
| Row address hold time | tRAH | 8 | | 8 | | ns | 11 |
| Column address set-up time | tASC | 0 | | 0 | | ns | |
| Column address hold time | tCAH | 10 | | 10 | | ns | |
| Column address to RAS lead time | tRAL | 30 | | 35 | | ns | 11 |
| Read command set-up time | tRCS | 0 | | 0 | | ns | |
| Read command hold referencde to CAS | tRCH | 0 | | 0 | | ns | 8 |
| Read command hold referenced to RAS | tRRH | -2 | | -2 | | ns | 8,11 |
| Write command hold time | tWCH | 10 | | 10 | | ns | |
| Write command pulse width | tWP | 10 | | 10 | | ns | |
| Write command to RAS lead time | tRWL | 20 | | 20 | | ns | 11 |
| Write command to CAS lead time | tCWL | 13 | | 15 | | ns | |
| Data in set-up time | tDS | -2 | | -2 | | ns | 9,11 |
| Data in hold time | tDH | 15 | | 15 | | ns | 9,11 |
| Refresh period(4K & 8K) | tREF | | 64 | | 64 | ms | |
| Write command set-up time | tWCS | 0 | | 0 | | ns | 7 |
| CAS to W delay time | tCWD | 36 | | 40 | | ns | 7 |
| Column address to W delay time | tAWD | 48 | | 55 | | ns | 7 |
| CAS prechange to W delay time | tCPWD | 53 | | 60 | | ns | 7 |

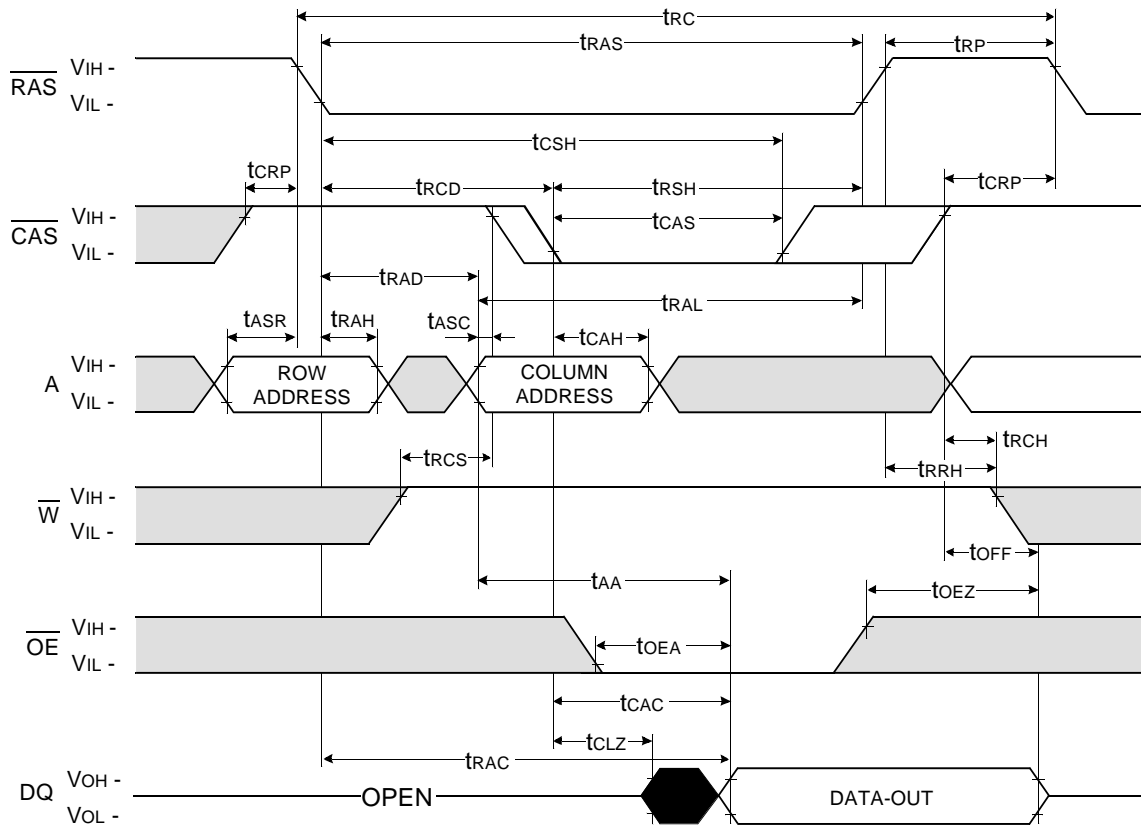
AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

| Parameter | Symbol | -5 | | -6 | | Unit | Note |
|---|--------------------|-----|------|-----|------|------|------|
| | | Min | Max | Min | Max | | |
| RAS to W delay time | t _{RWD} | 71 | | 83 | | ns | 7,11 |
| CAS setup time(CAS-before-RAS refresh) | t _{CSR} | 10 | | 10 | | ns | 11 |
| CAS hold time(CAS-before-RAS refresh) | t _{CHR} | 8 | | 8 | | ns | 11 |
| RAS to CAS precharge time | t _{RPC} | 3 | | 3 | | ns | 11 |
| Access time from CAS precharge | t _{CPA} | | 35 | | 40 | ns | 3,11 |
| Fast page mode cycle time | t _{PC} | 35 | | 40 | | ns | |
| Fast page mode read-modify-write cycle time | t _{PRWC} | 76 | | 85 | | ns | |
| CAS precharge time(Fast page cycle) | t _{CP} | 10 | | 10 | | ns | |
| RAS pulse width(Fast page cycle) | t _{RASP} | 50 | 200K | 60 | 200K | ns | |
| RAS hold time from CAS precharge | t _{RHCP} | 35 | | 40 | | ns | 11 |
| W to RAS precharge time(C-B-R refresh) | t _{WRP} | 15 | | 15 | | ns | 11 |
| W to RAS hold time(C-B-R refresh) | t _{WRH} | 8 | | 8 | | ns | 11 |
| OE access time | t _{OEA} | | 18 | | 20 | ns | 11 |
| OE to data delay | t _{OED} | 18 | | 20 | | ns | 11 |
| Output buffer turn off delay time from OE | t _{OEZ} | 5 | 18 | 5 | 20 | ns | 11 |
| OE command hold time | t _{OEH} | 13 | | 15 | | ns | |
| Present Detect Read Cycle | | | | | | | |
| PDE to Valid PD bit | t _{PD} | | 10 | | 10 | ns | |
| PDE to PD bit Inactive | t _{PDOFF} | 2 | 7 | 2 | 7 | ns | |

NOTES

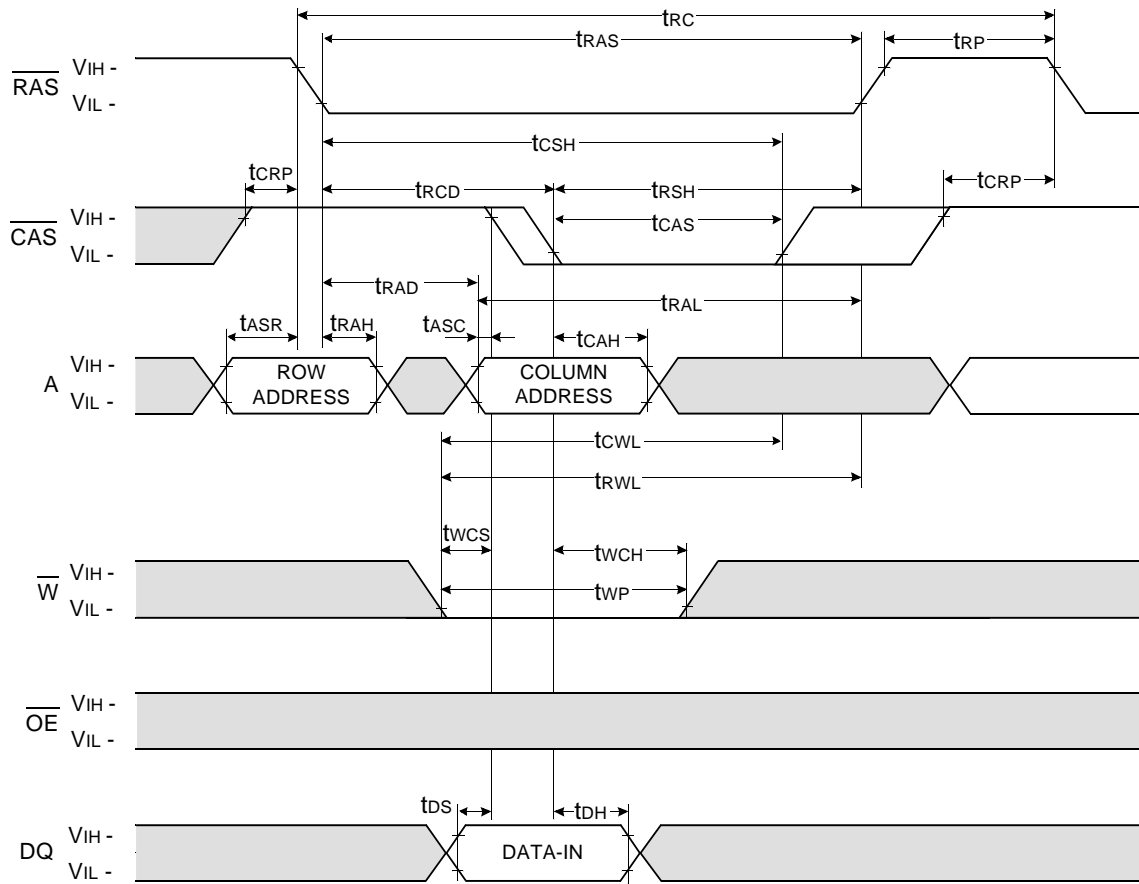
1. An initial pause of 200us is required after power-up followed by any 8 RAS-only or CAS-before-RAS refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{IH}/V_{IL}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF.
4. Operation within the t_{RCD}(max) limit insures that t_{TRAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes tha t_{RCD}≥t_{RCD}(max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. twcs, t_{RWD}, t_{CPWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If twcs≥twcs(min) the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If t_{RWD}≥t_{RWD}(min), t_{CPWD}≥t_{CPWD}(min), t_{AWD}≥t_{AWD}(min) and t_{CPWD}≥t_{CPWD}(min). The cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out(at access time) is indeterminate.
8. Either t_{TRCH} or t_{TRRH} must be satisfied for a read cycle.
9. These parameters are referenced to the CAS leading edge in early write cycles.
10. Operation within the t_{TRAD}(max) limit insures that t_{TRAC}(max) can be met. t_{TRAD}(max) is specified as reference point only. If t_{TRAD} is greater than the specified t_{TRAD}(max) limit, then access time is controlled by t_{AA}.
11. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

READ CYCLE



WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

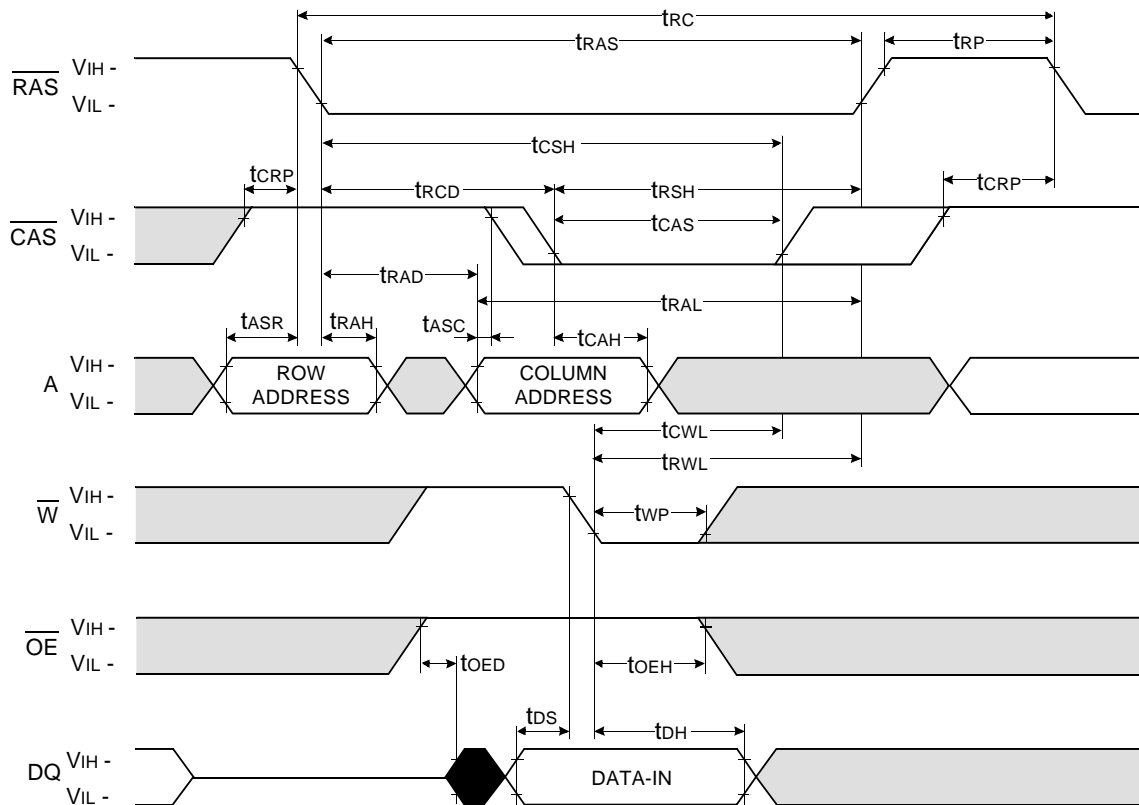


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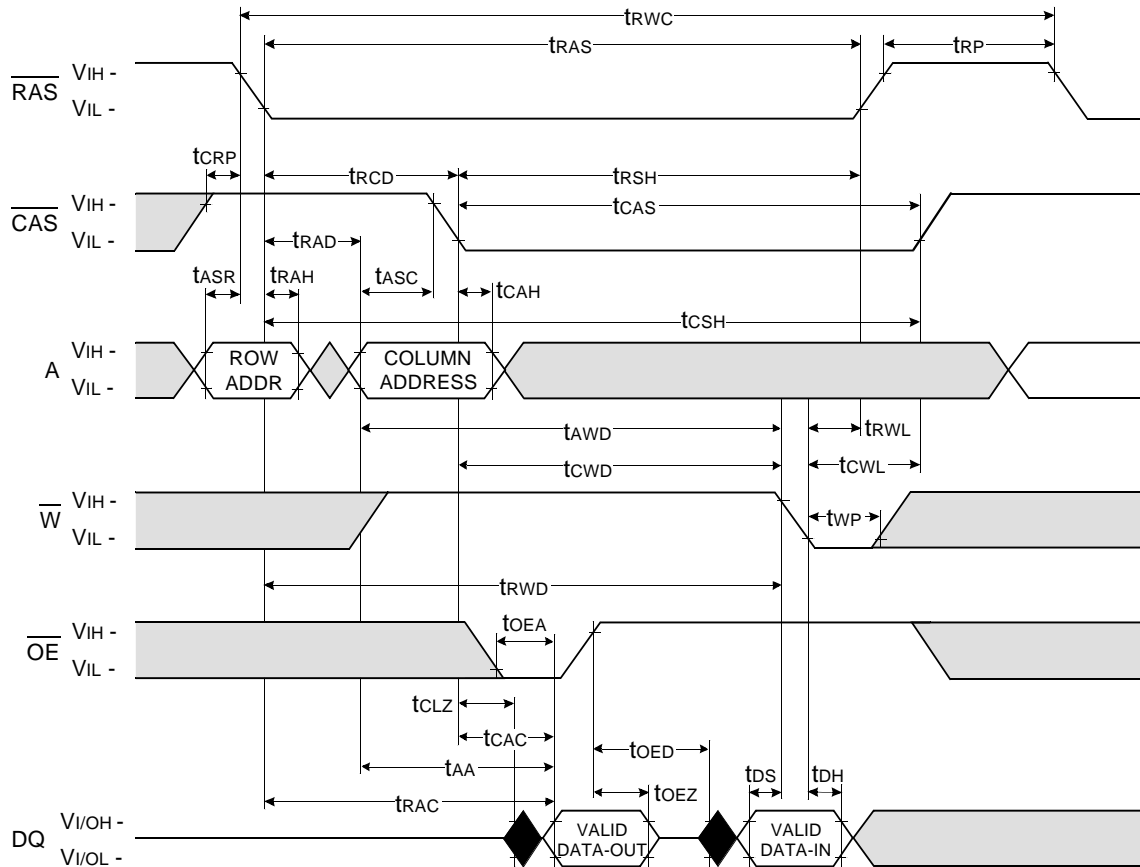
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : DOUT = OPEN



Don't care
Undefined

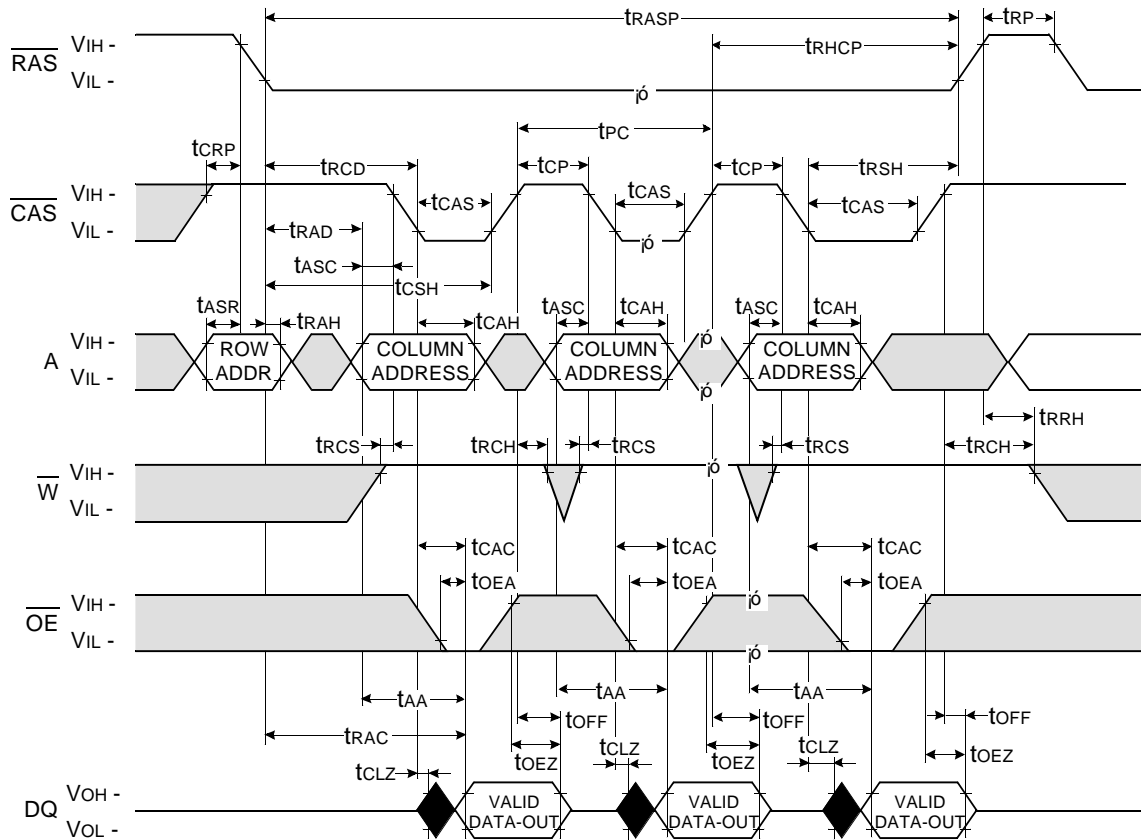
READ - MODIFY - WRITE CYCLE



Don't care
Undefined

FAST PAGE READ CYCLE

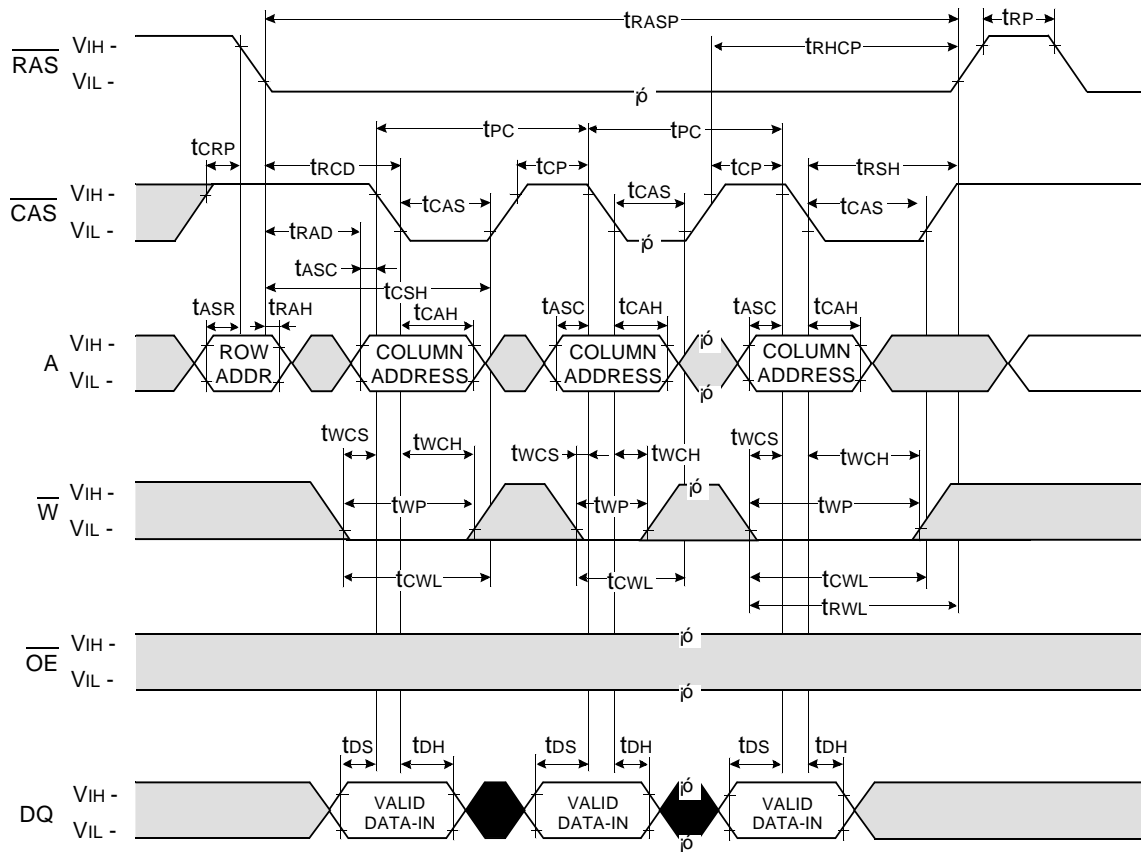
NOTE : DOUT = OPEN



Don't care
Undefined

FAST PAGE WRITE CYCLE (EARLY WRITE)

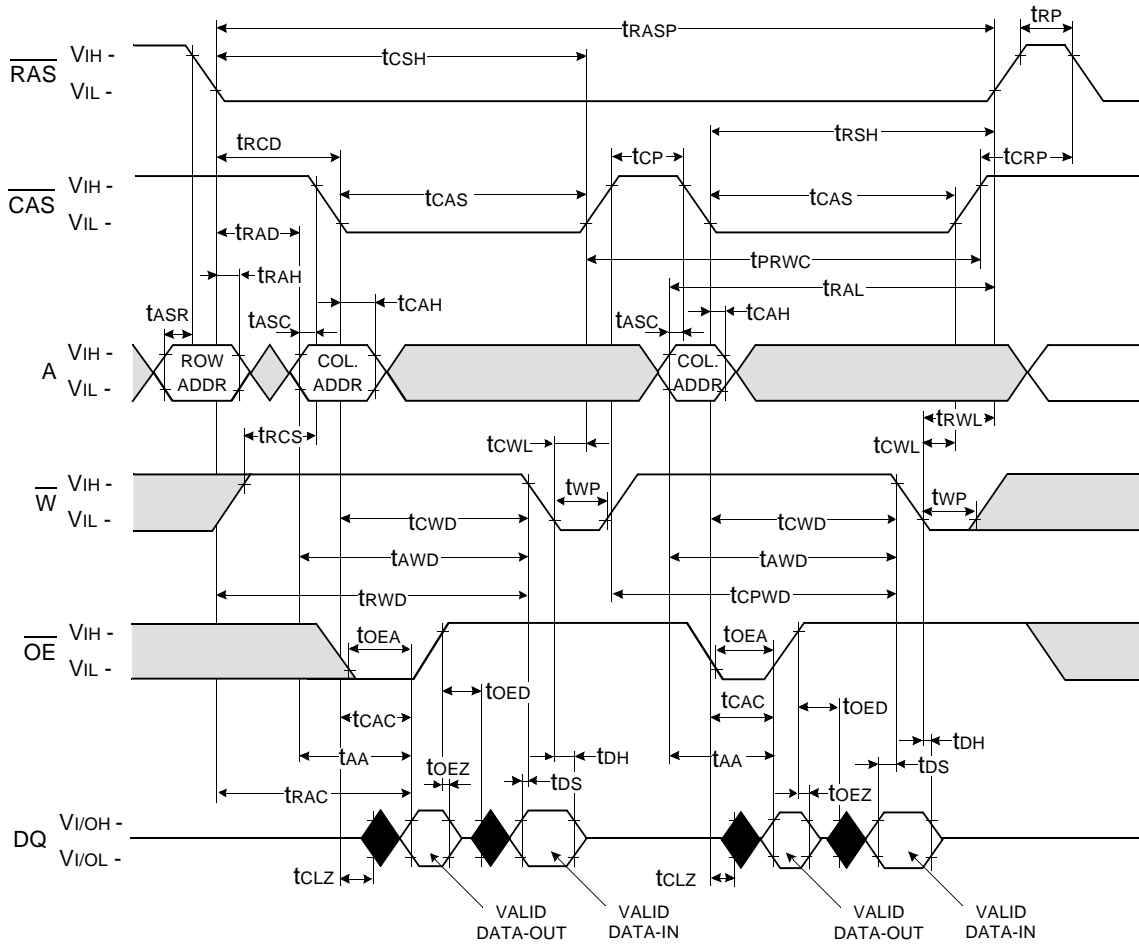
NOTE : DOUT = OPEN



Don't care

Undefined

FAST PAGE READ - MODIFY - WRITE CYCLE

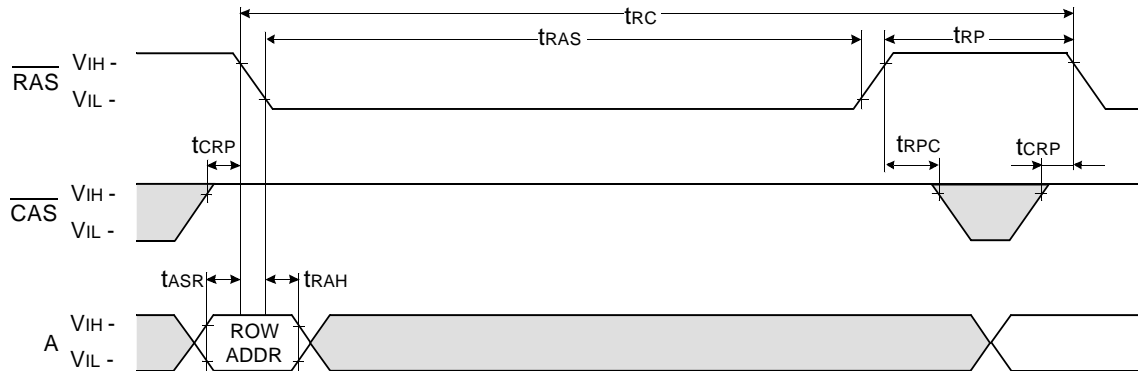


Don't care
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$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE

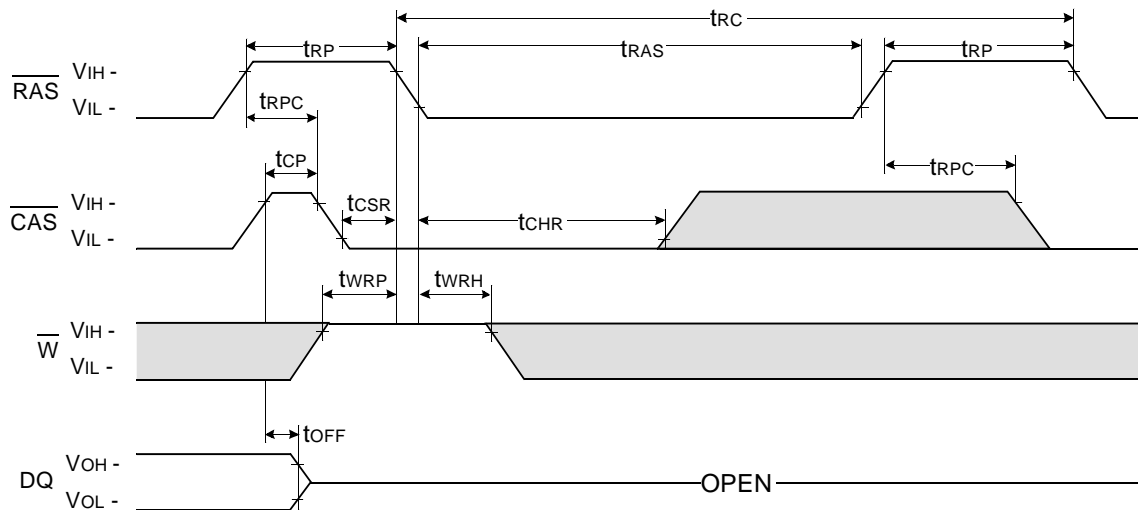
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

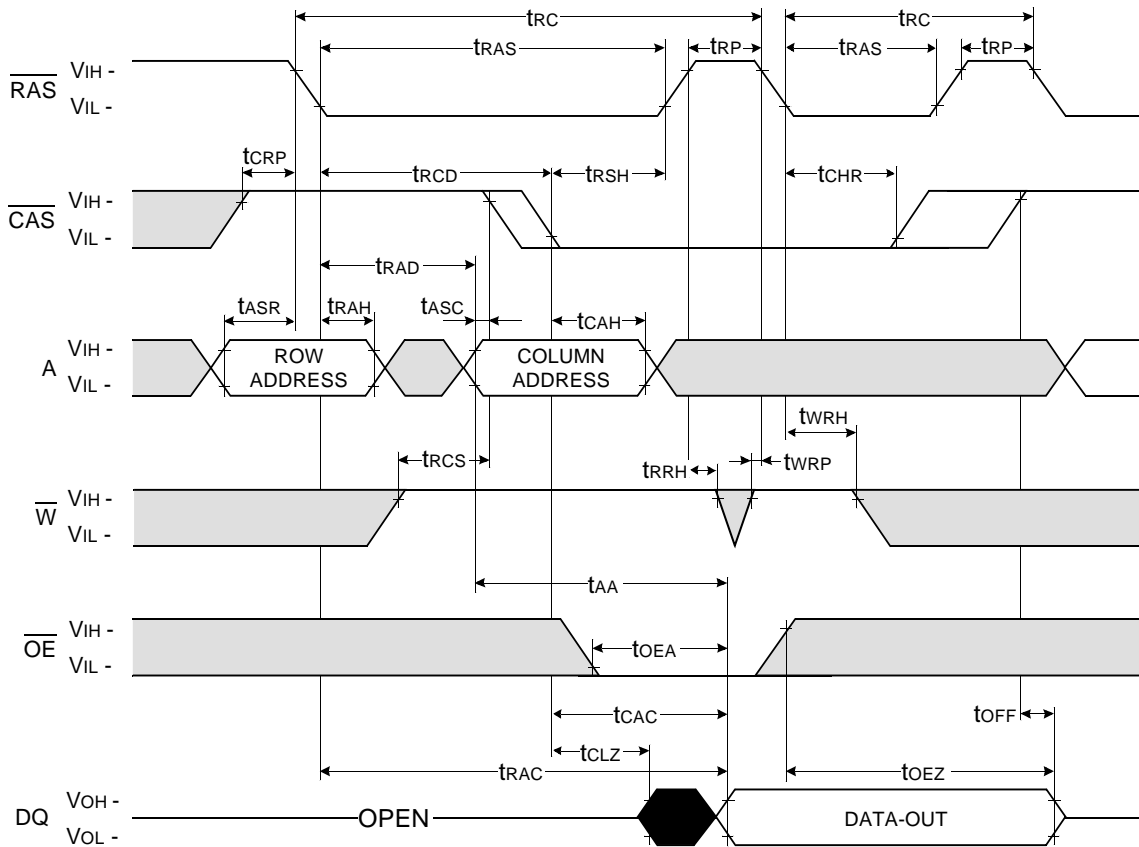
NOTE : $\overline{\text{OE}}$, A = Don't care



Don't care

Undefined

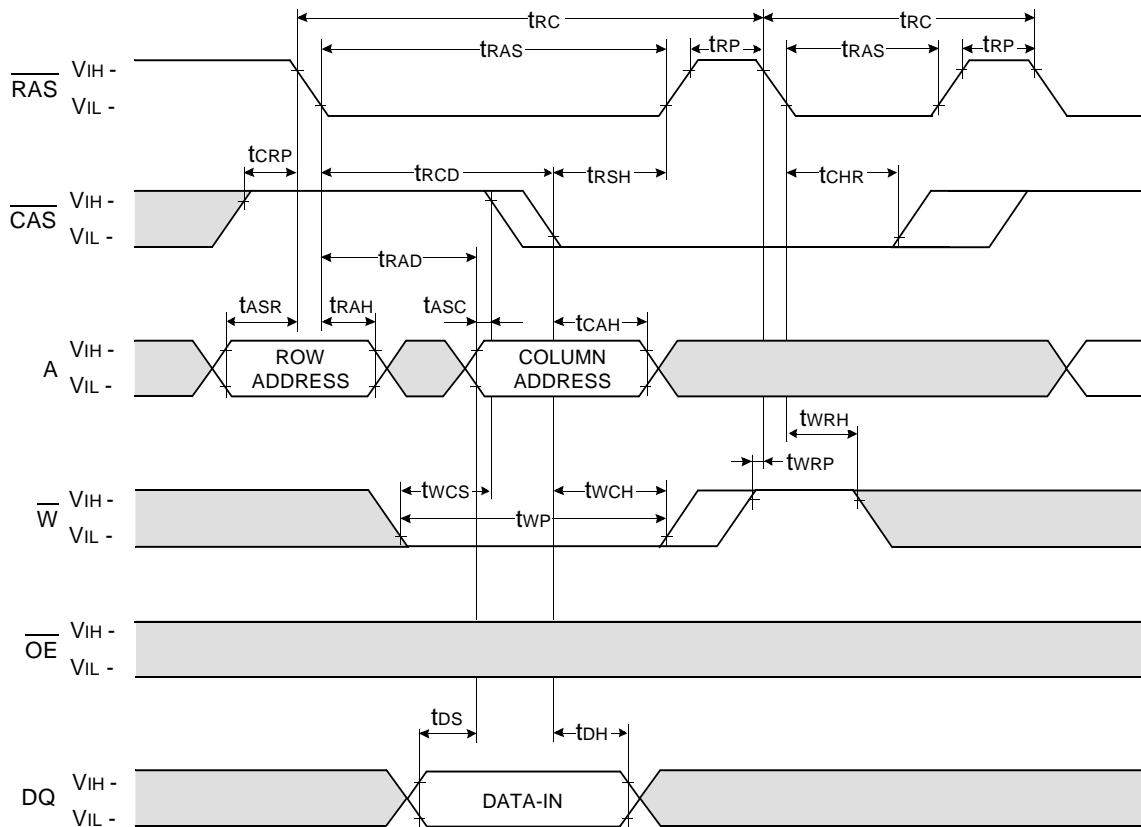
HIDDEN REFRESH CYCLE (READ)



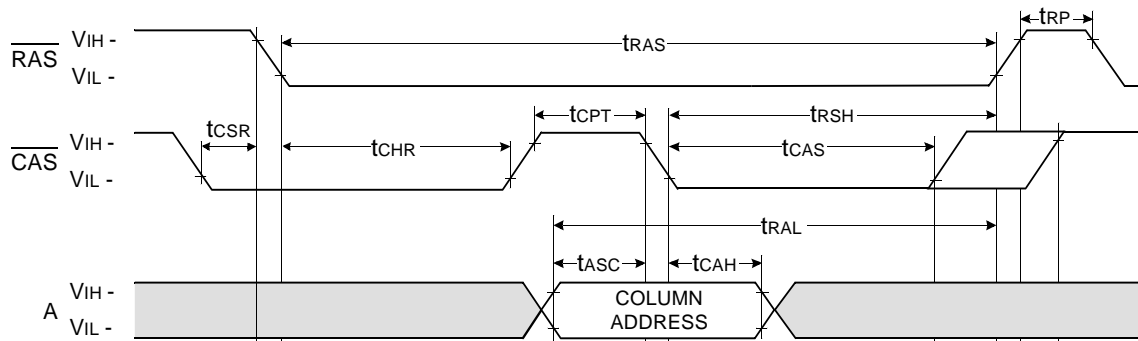
Don't care
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HIDDEN REFRESH CYCLE (WRITE)

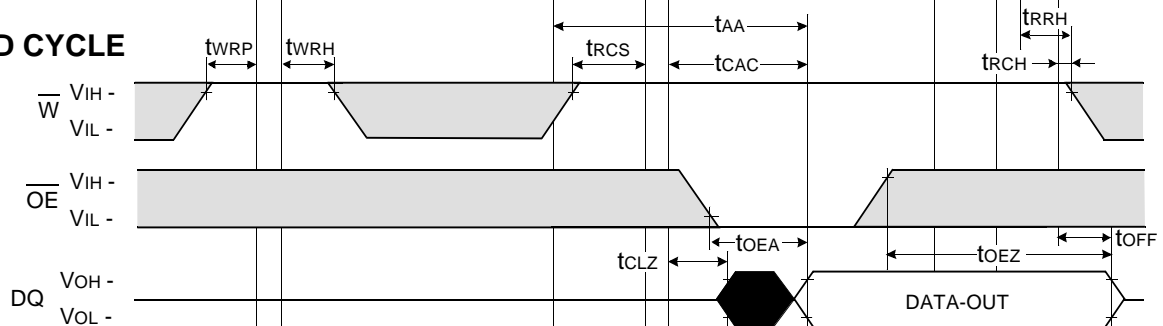
NOTE : DOUT = OPEN



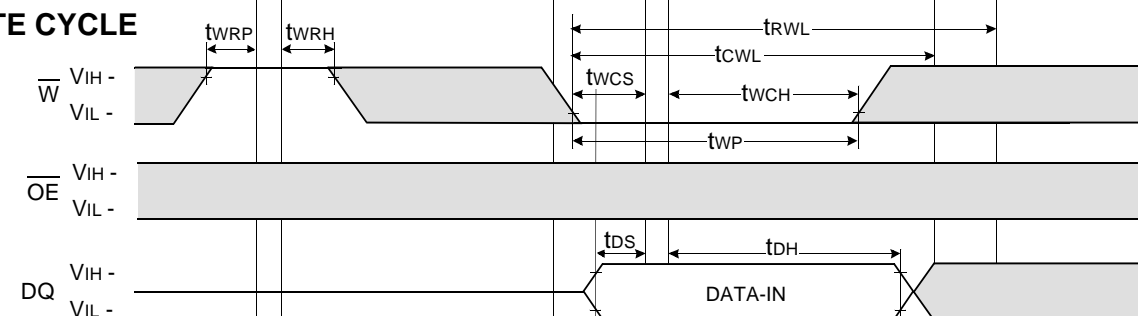
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



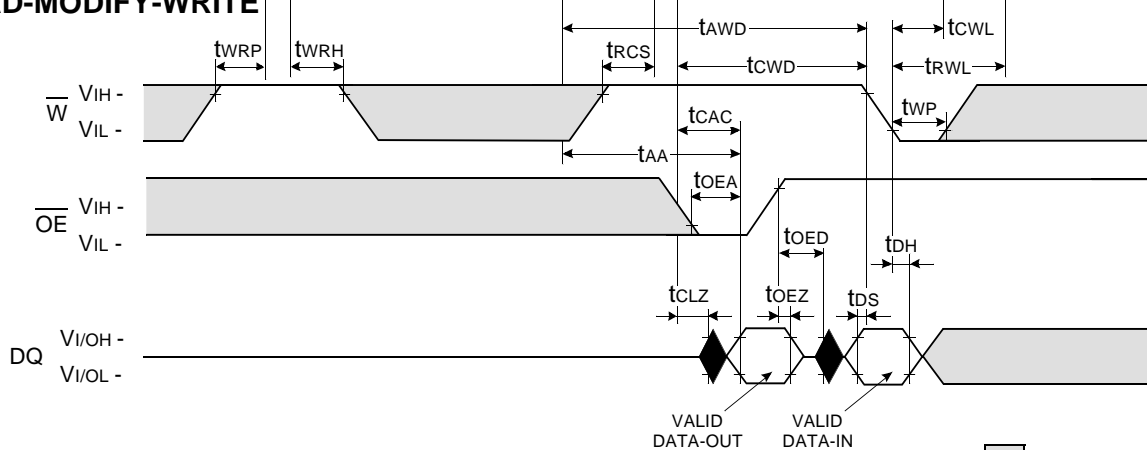
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE



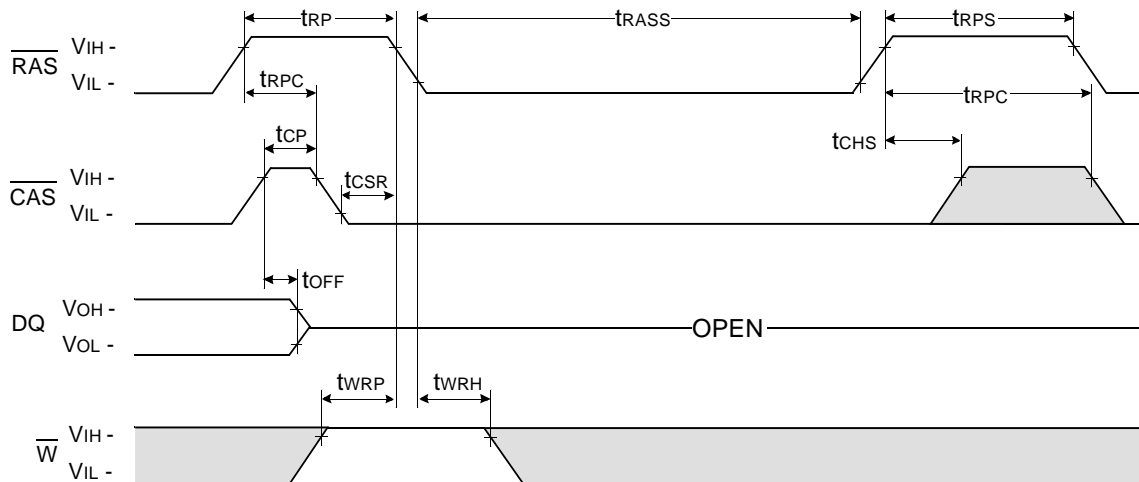
Don't care

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NOTE : This timing diagram is applied to all devices besides 16M DRAM 4th & 64M DRAM.

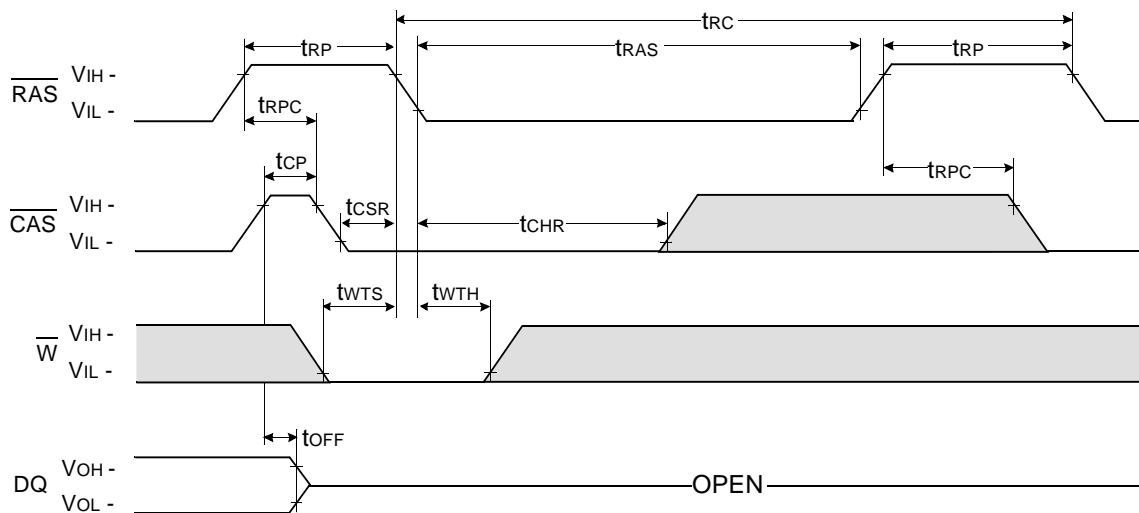
$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ SELF REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



TEST MODE IN CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



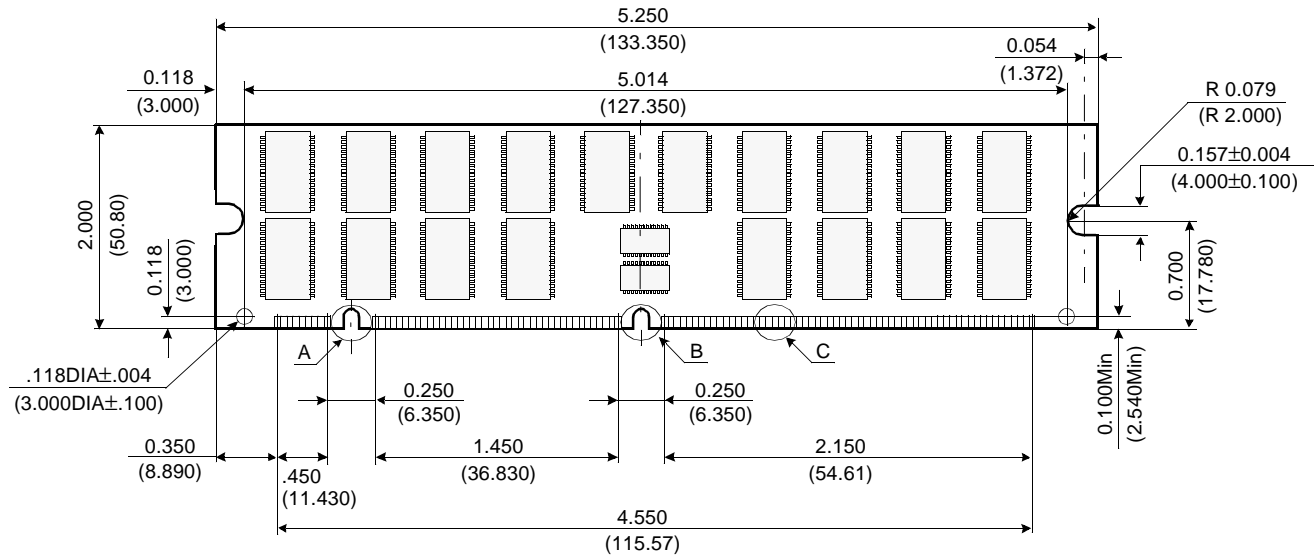
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DRAM MODULE

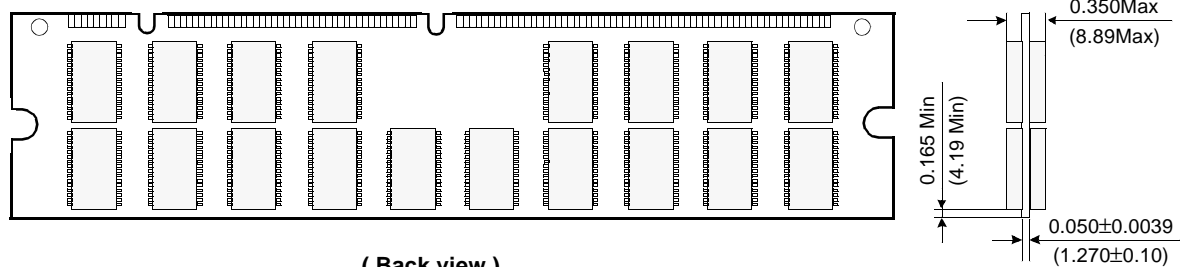
KMM372V320(8)0CK4

PACKAGE DIMENSIONS

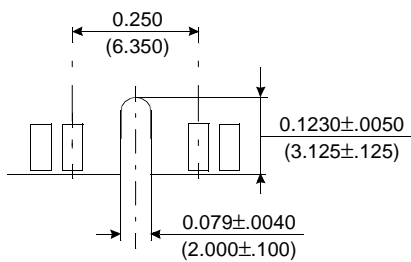
Units : Inches (millimeters)



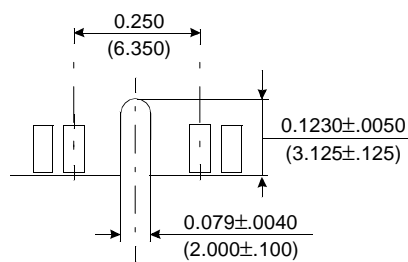
(Front view)



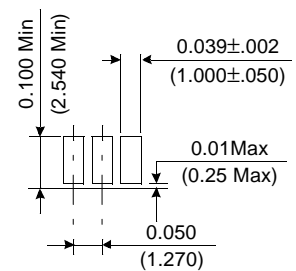
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 16Mx4 DRAM with Fast Page mode, SOJ
 DRAM Part No. : KMM372V3200CK4 - KM44V16100CK.
 KMM372V3280CK4 - KM44V16000CK.