April 1998

FAIRCHILD SEMICONDUCTOR™

DM74LS469
8-Bit Up/Down Counter

General Description

The 'LS469 is an 8-bit synchronous up/down counter with parallel load and hold capability. Three function-select inputs ($\overline{LD}$, $\overline{UD}$, $\overline{CBI}$) provide one of four operations which occur synchronously on the rising edge of the clock (CK).

The LOAD operation loads the inputs (D_7–D_0) into the output register (Q_7–Q_0). The HOLD operation holds the previous value regardless of clock transitions. The INCREMENT operation adds one to the output register when the carry-in input is TRUE ($\overline{CBI}$ =LOW), otherwise the operation is a HOLD. The carry-out ($\overline{CBO}$) is TRUE ($\overline{CBO}$ =LOW) when the output register (Q_7–Q_0) is all HIGHs, otherwise FALSE ($\overline{CBO}$ =HIGH). The DECREMENT operation subtracts one from the output register when the borrow-in input is TRUE ($\overline{CBI}$ =LOW), otherwise the operation is a HOLD. The borrow-out ($\overline{CBO}$) is TRUE ($\overline{CBO}$ =LOW) when the output register (Q_7–Q_0) is all LOWs, otherwise FALSE ($\overline{CBO}$ =HIGH).

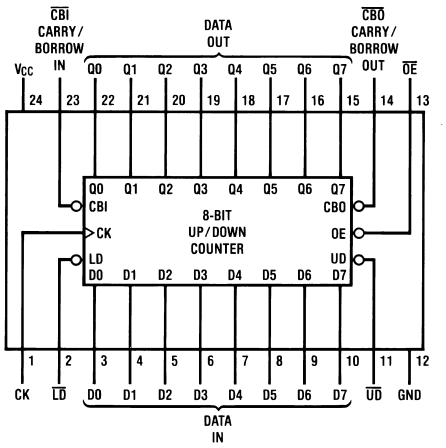
The output register (Q_7–Q_0) is enabled when $\overline{OE}$ is LOW, and disabled (HI-Z) when $\overline{OE}$ is HIGH. The output drivers will sink the 24 mA required for many bus-interface standards. Two or more 'LS469 octal up/down counters may be cascaded to provide larger counters.

Features/Benefits

- 8-bit up/down counter for microprogram-counter, DMA controller and general-purpose counting applications
- 8 bits matches byte boundaries
- Bus-structured pinout
- 24-pin SKINNYDIP saves space
- 3-STATE outputs drive bus lines
- Low current PNP inputs reduce loading
- Expandable in 8-bit increments

Connection Diagram

Top View



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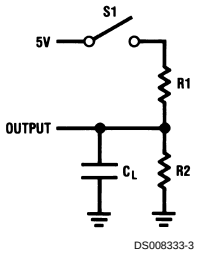
Order Number DM54LS469J,
DM74LS469J or DM74LS469N
See Package Number J24F or N24C

Standard Test Load



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Function Table

$\overline{OE}$	CK	$\overline{LD}$	$\overline{UD}$	$\overline{CBI}$	D7–D0	Q7–Q0	Operation
H	X	X	X	X	X	Z	HI-Z
L	↑	L	X	X	D	D	LOAD
L	↑	H	L	H	X	Q	HOLD
L	↑	H	L	L	X	Q plus 1	INCREMENT
L	↑	H	H	H	X	Q	HOLD
L	↑	H	H	L	X	Q minus 1	DECREMENT

Absolute Maximum Ratings (Note 1)

Supply Voltage V_{CC}	7V
Input Voltage	5.5V
Off-State Output Voltage	5.5V
Storage Temperature	−65˚C to +150˚C

Operating Conditions

Symbol	Parameter		Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature		−55		125 (Note 2)	0		75	˚C
t_W	Width of Clock	Low	40			35	10		ns
		High	30			25			
t_{SU}	Set Up Time		60			50			ns
t_h	Hold Time		0	−15		0	−15		

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits.

Note 2: Case Temperature

Electrical Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions			Min	Typ (Note 4)	Max	Units
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IH}	High-Level Input Voltage				2			V
V_{IC}	Input Clamp Voltage	V_{CC}=MIN	I_I=−18 mA				−1.5	V
I_{IL}	Low-Level Input Current	V_{CC}=MAX	V_I=0.4V				−0.25	mA
I_{IH}	High-Level Input Current	V_{CC}=MAX	V_I=2.4V				25	µA
I_I	Maximum Input Current	V_{CC}=MAX	V_I=5.5V				1	mA
V_{OL}	Low-Level Output Voltage	V_{CC}=MIN V_{IL}=0.8V	MIL	I_{OL}=12 mA			0.5	V
		V_{IH}=2V	COM	I_{OL}=24 mA				
V_{OH}	High-Level Output Voltage	V_{CC}=MIN V_{IL}=0.8V	MIL	I_{OH}=−2 mA	2.4			V
		V_{IH}=2V	COM	I_{OH}=−3.2 mA				
I_{OZL}	Off-State Output Current	V_{CC}=MAX V_{IL}=0.8V		V_O=0.4V			−100	µA
I_{OZH}		V_{IH}=2V		V_O=2.4V			100	µA
I_{OS}	Output Short-Circuit Current (Note 3)	V_{CC}=5.0V		V_O=0V	−30		−130	mA
I_{CC}	Supply Current	V_{CC}=MAX				120	180	mA

Note 3: No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

Note 4: All typical values are V_{CC}=5V, T_A=25˚C.

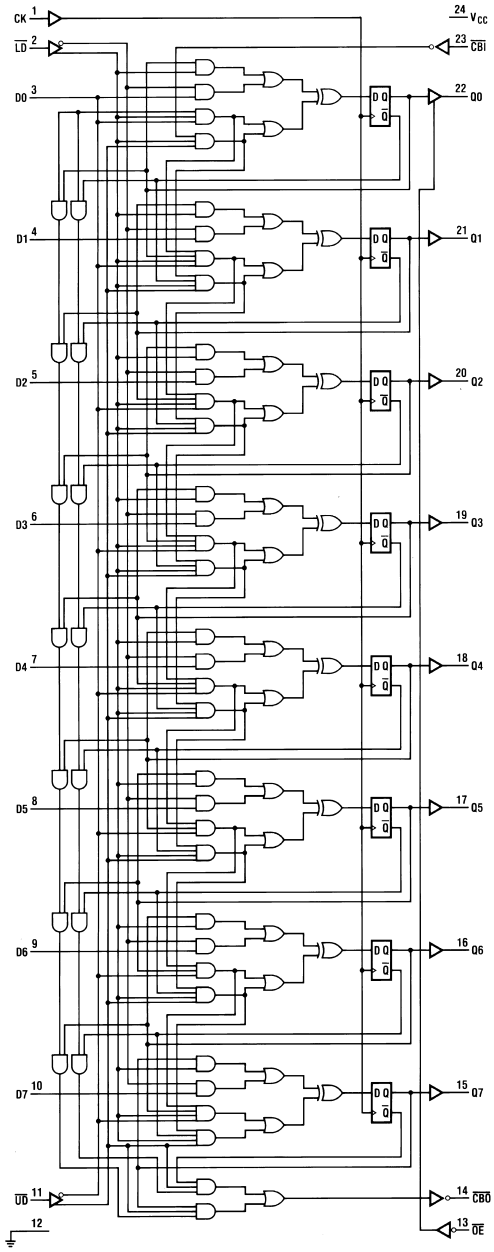
Switching Characteristics

Over Operating Conditions

Symbol	Parameter	Test Conditions (See Test Load/Waveforms)	Military			Commercial			Units
			Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Clock Frequency		10.5			12.5			MHz
t_{PD}	$\overline{CBI}$ to $\overline{CBO}$ Delay	C_L=50 pF		35	60		35	50	ns
t_{PD}	Clock to Q	R_1=200Ω		20	35		20	30	ns
t_{PD}	Clock to CBO	R_2=390Ω		55	95		55	80	ns
t_{PZX}	Output Enable Delay			20	45		20	35	ns
t_{PXZ}	Output Disable Delay			20	45		20	35	ns

Logic Diagram

LS469



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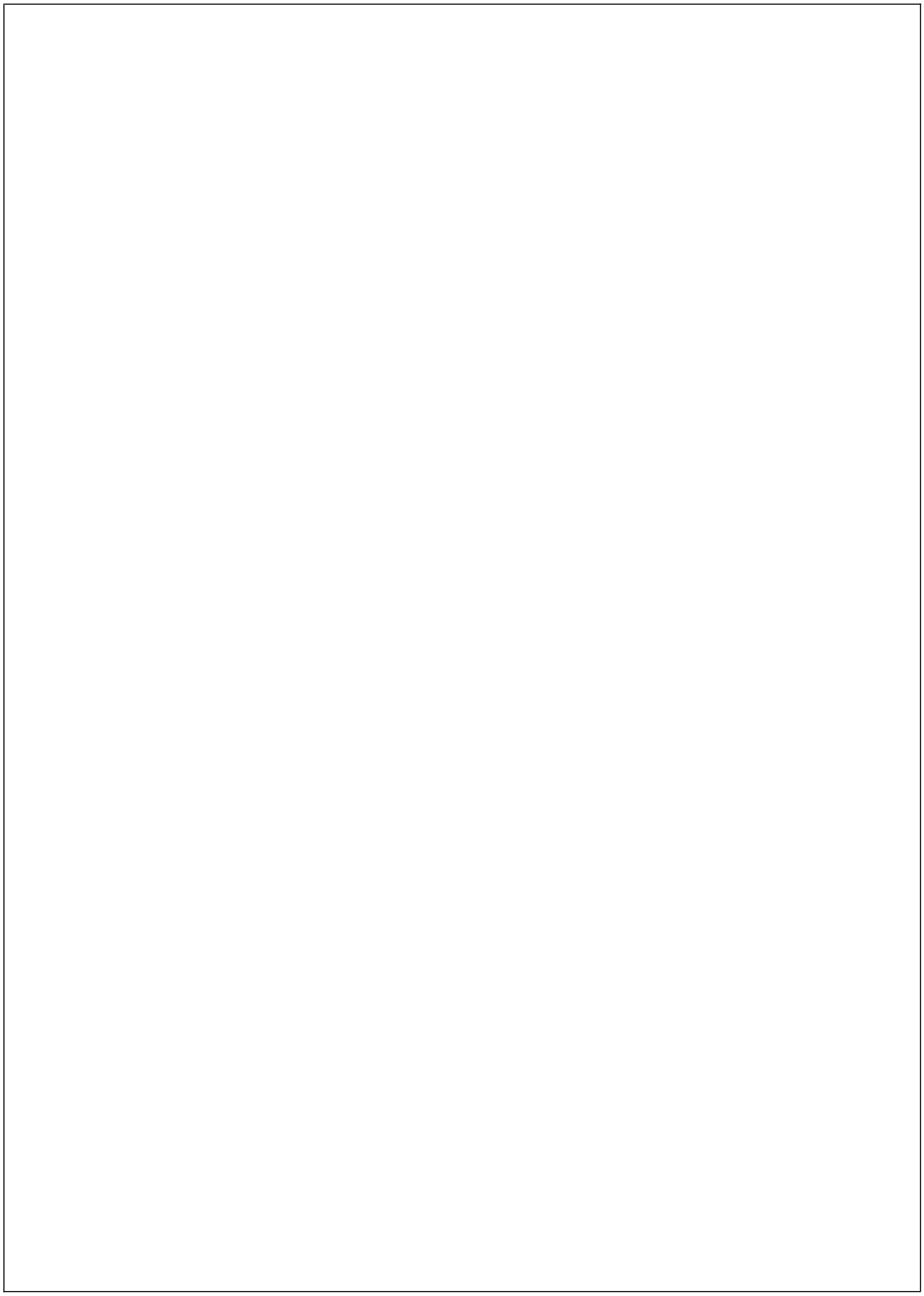
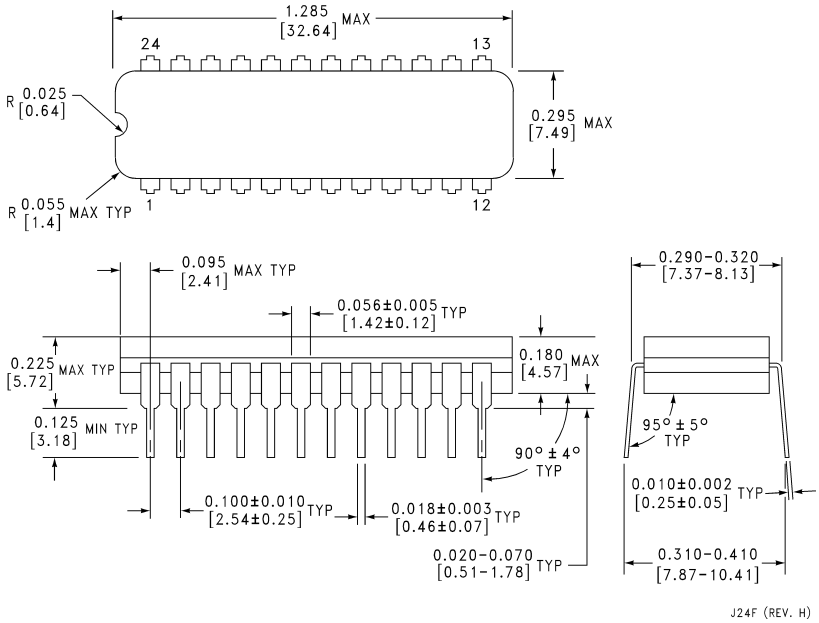
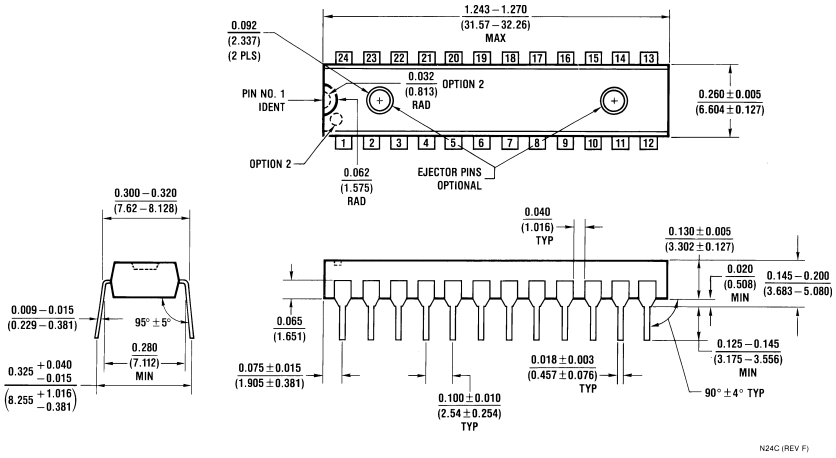


Physical Dimensions inches (millimeters) unless otherwise noted



24-Pin Narrow Ceramic Dual-In-Line Package (J)
Order Number DM54LS469J or DM74LS469J
Package Number J24F



24-Pin Narrow Plastic Dual-In-Line Package (N)
Order Number DM74LS469N
Package Number N24C

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