



## X0402BE – X0402NE SCR'S

**4.0 A 200–800 V <200  $\mu$ A**

The X0402 series silicon controlled rectifiers are high performance PNP devices diffused with TAG's proprietary Top Glass™ Process. These parts are intended for general purpose applications where gate sensitivity is required.

### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Part Nr.	Symbol	Min.	Max.	Unit	Test Conditions
Repetitive Peak Off State Voltage	<b>X0402BE</b>		200		V	
	<b>X0402DE</b>	$V_{DRM}$	400		V	$T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$
	<b>X0402ME</b>	$V_{RRM}$	600		V	$R_{GK} = 1\text{K}\Omega$
	<b>X0402NE</b>		800		V	
On-State Current		$I_{T(RMS)}$	4.0		A	All Conduction Angles $T_C = 85^\circ\text{C}$
Average On-State Current		$I_{T(AV)}$	2.5		A	Half Cycle, $\Theta = 180^\circ$ , $T_C = 85^\circ\text{C}$
Nonrept. On-State Current		$I_{TSM}$	33		A	Half Cycle, 60 Hz
Nonrept. On-State Current		$I_{TSM}$	30		A	Half Cycle, 50 Hz
Fusing Current		$I^2t$	4.5		$\text{A}^2\text{s}$	$t = 10\text{ ms}$ , Half Cycle
Peak Reverse Gate Voltage		$V_{GRM}$	8		V	$I_{GR} = 10\text{ }\mu\text{A}$
Peak Gate Current		$I_{GM}$	1.2		A	$10\text{ }\mu\text{s}$ max.
Peak Gate Dissipation		$P_{GM}$	3		W	$10\text{ }\mu\text{s}$ max.
Gate Dissipation		$P_{G(AV)}$	0.2		W	$20\text{ ms}$ max.
Operating Temperature		$T_J$	-40	125	$^\circ\text{C}$	
Storage Temperature		$T_{stg}$	-40	150	$^\circ\text{C}$	
Soldering Temperature		$T_{sld}$		250	$^\circ\text{C}$	$1.6\text{ mm}$ from case, $10\text{ s}$ max.

### Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Off-State Leakage Current	$I_{DRM}/I_{RRM}$		0.2	mA	@ $V_{DRM} + V_{RRM}$ , $R_{GK} = 1\text{K}\Omega$ , $T_J = 125^\circ\text{C}$
Off-State Leakage Current	$I_{DRM}/I_{RRM}$		5	$\mu\text{A}$	@ $V_{DRM} + V_{RRM}$ , $R_{GK} = 1\text{K}\Omega$ , $T_J = 25^\circ\text{C}$
On-State Voltage	$V_T$		2.11	V	at $I_T = 8\text{ A}$ , $T_J = 25^\circ\text{C}$
On-State Threshold Voltage	$V_{T(TO)}$		1.05	V	$T_J = 125^\circ\text{C}$
On-State Slope Resistance	$r_T$		150	m $\Omega$	$T_J = 125^\circ\text{C}$
Gate Trigger Current	$I_{GT}$		200	$\mu\text{A}$	$V_D = 7\text{ V}$
Gate Trigger Voltage	$V_{GT}$		0.8	V	$V_D = 7\text{ V}$
Holding Current	$I_H$		5	mA	$R_{GK} = 1\text{K}\Omega$
Latching Current	$I_L$		6	mA	$R_{GK} = 1\text{K}\Omega$
Critical Rate of Voltage Rise	$dv/dt$	30		V/ $\mu\text{s}$	$V_D = .67 \times V_{DRM}$ , $R_{GK} = 1\text{K}\Omega$ , $T_J = 125^\circ\text{C}$
Critical Rate of Current Rise	$di/dt$	50		A/ $\mu\text{s}$	$I_G = 10\text{ mA}$ , $di_G/dt = 0.1\text{ A}/\mu\text{s}$ , $T_J = 125^\circ\text{C}$
Gate Controlled Delay Time	$t_{gd}$		2	$\mu\text{s}$	$I_G = 10\text{ mA}$ , $di_G/dt = 0.1\text{ A}/\mu\text{s}$
Commutated Turn-Off Time	$t_q$		50	$\mu\text{s}$	$T_C = 85^\circ\text{C}$ , $V_D = .67 \times V_{DRM}$ , $V_R = 35\text{ V}$ , $I_T = I_{T(AV)}$
Thermal Resistance junc. to case	$R_{\theta jc}$		7.5	K/W	
Thermal Resistance junc. to amb.	$R_{\theta ja}$		75	K/W	