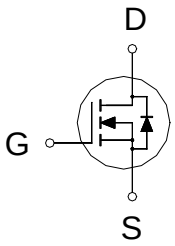
杰力科技股份有限公司
Excelliance MOS Corporation

EMD09N08H

N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	80V
$R_{DSON\ (MAX.)}$	9mΩ
I_D	56A





UIS, Rg 100% Tested

Pb-Free Lead Plating

GP
GREEN PRODUCT

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_C = 25 °C	I_D	56	A
	T_C = 100 °C		38	
Pulsed Drain Current[1]		I_{DM}	170	
Avalanche Current		I_{AS}	45	
Avalanche Energy	L = 0.3mH, ID=45A, RG=25Ω	E_{AS}	303	mJ
Repetitive Avalanche Energy[2]	L = 0.1mH	E_{AR}	101	
Power Dissipation	T_C = 25 °C	P_D	50	W
	T_C = 100 °C		20	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2.5	°C / W
Junction-to-Ambient	$R_{\theta JA}$		50	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	80			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	2.0	3.0	4.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±25V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V			1	μA
		V_{DS} = 50V, V_{GS} = 0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	56			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 30A		7.5	9	mΩ
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 30A		40		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		3905		pF
Output Capacitance	C_{oss}			378		
Reverse Transfer Capacitance	C_{rss}			363		
Gate Resistance	R_g	V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz		2.5		Ω
Total Gate Charge[1,2]	Q_g	V_{DS} = 40V, V_{GS} = 10V, I_D = 30A		64		nC
Gate-Source Charge[1,2]	Q_{gs}			19		
Gate-Drain Charge[1,2]	Q_{gd}			22		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 40V, I_D = 1A, V_{GS} = 10V, R_{GS} = 6Ω		30		nS
Rise Time[1,2]	t_r			200		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			100		
Fall Time[1,2]	t_f			150		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				56	A
Pulsed Current[3]	I_{SM}				170	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.3	V
Reverse Recovery Time	t_{rr}	I_F = 30A, dI_F/dt = 100A / μS		130		nS
Reverse Recovery Charge	Q_{rr}			400		nC

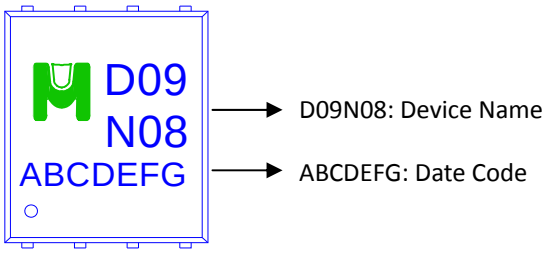
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

[2]Independent of operating temperature.

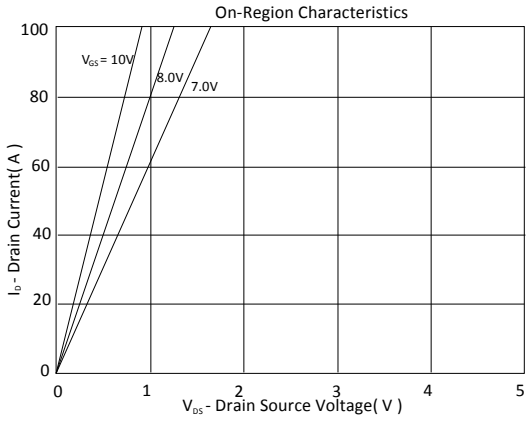
[3]Pulse width limited by maximum junction temperature.

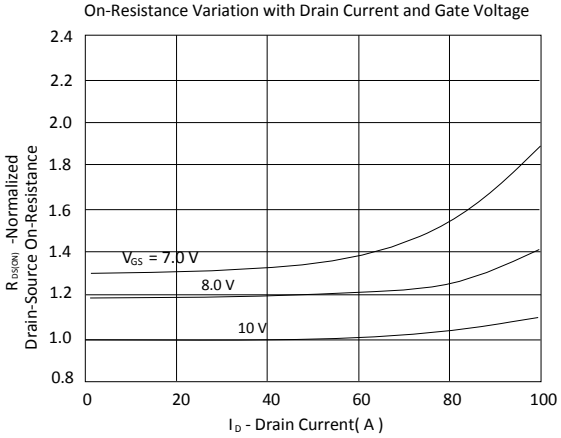
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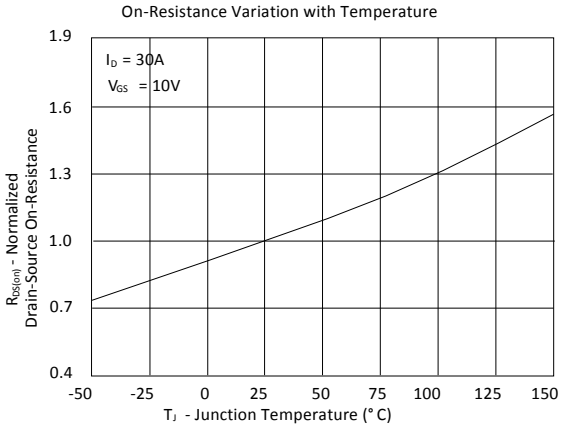
Device Name: EMD09N08H for EDFN 5 x 6

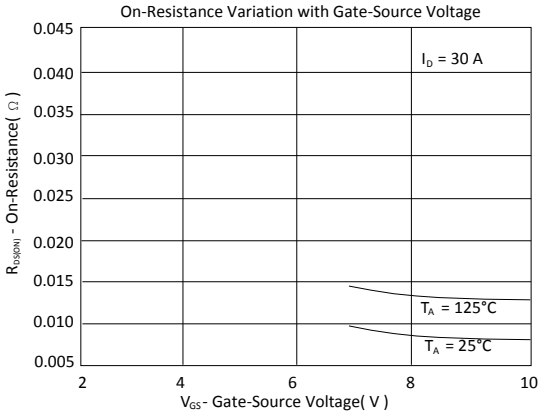


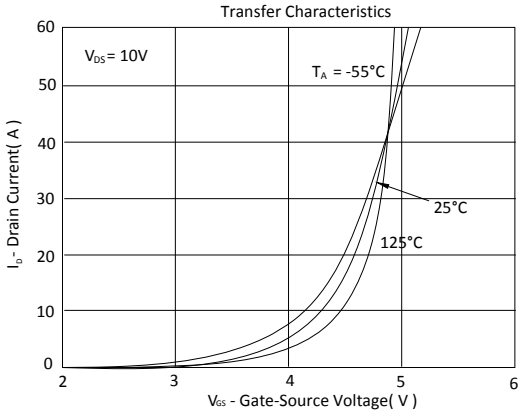
TYPICAL CHARACTERISTICS

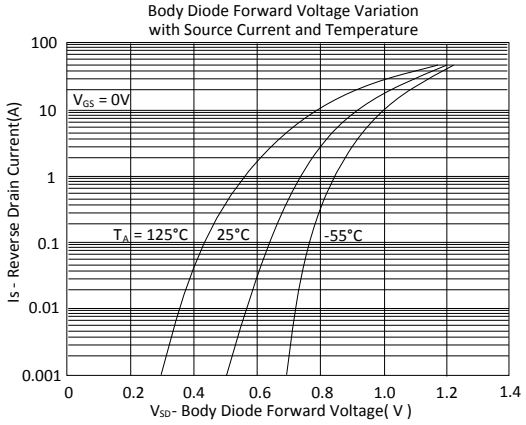




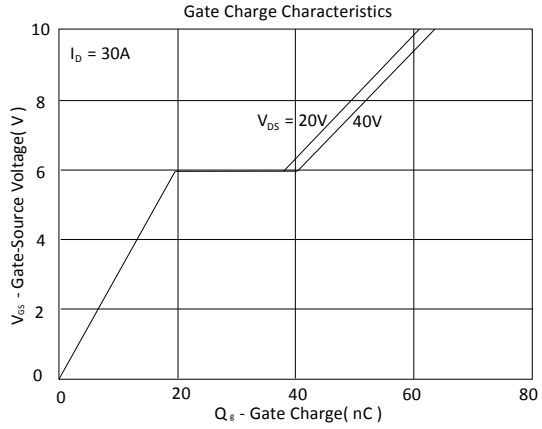




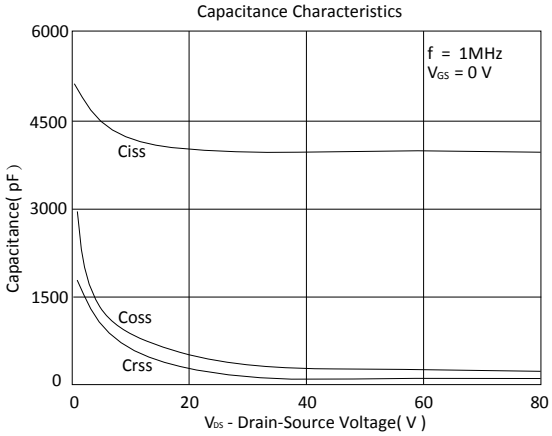




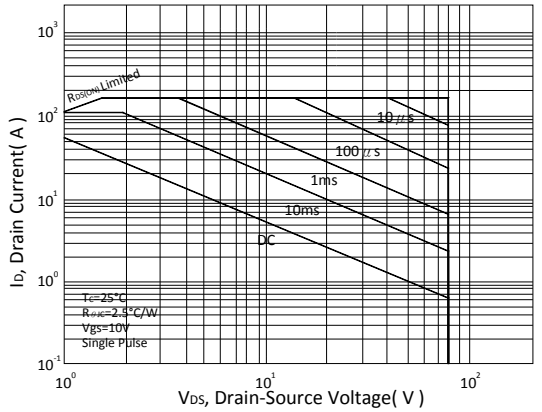
Gate Charge Characteristics



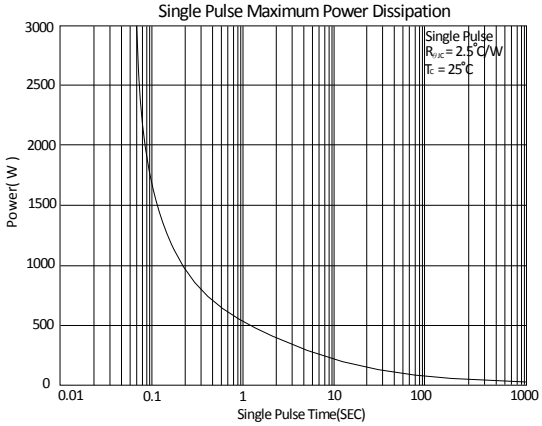
Capacitance Characteristics



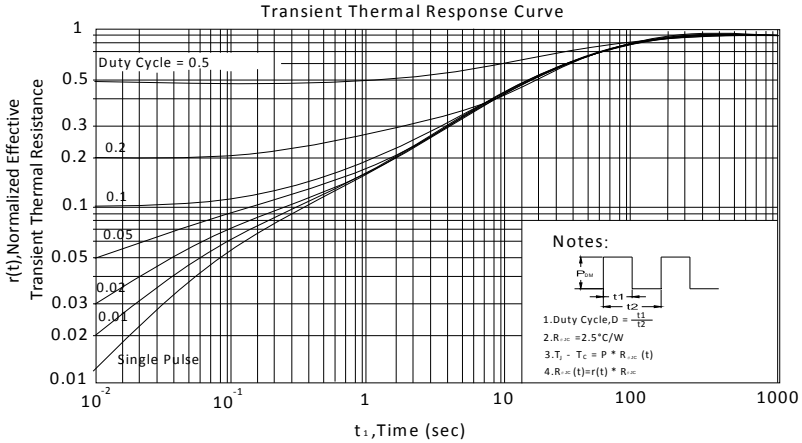
Maximum Safe Operating Area



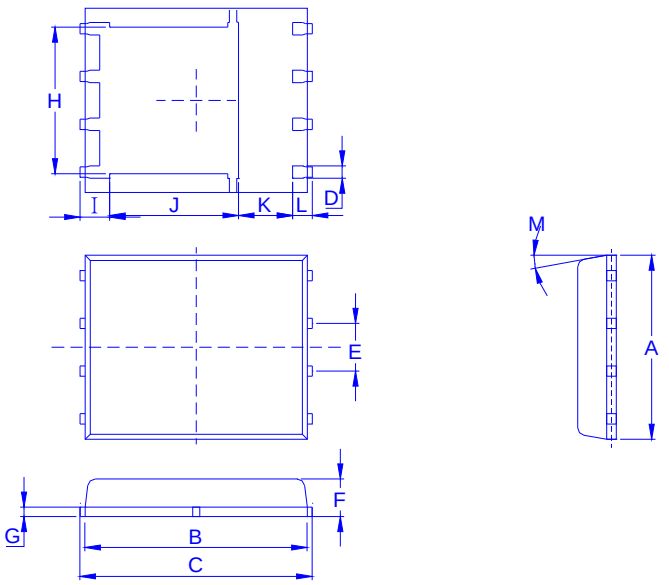
Single Pulse Maximum Power Dissipation



Transient Thermal Response Curve



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min.	4.80	5.50	5.90	0.3		0.85	0.15	3.67	0.41	3.00	0.94	0.45	0°
Typ.					1.27								
Max.	5.30	5.90	6.15	0.51		1.20	0.30	4.54	0.85	3.92	1.7	0.71	12°

Recommended minimum pads

